Josep Torrellas
Professor
Computer Science
University of Illinois at Urbana Champaign

Awards and honors and year received (list--no more than *five* items):

- IEEE Computer Society Technical Achievement Award. For ”Pioneering contributions to shared-memory multiprocessor architectures and thread-level speculation”, June 2015.
- High-Impact Paper Award, International Conference on Computer Design (ICCD). For ”One of the 5 most cited papers in the first 30 years of ICCD (1983-2012)”, October 2012.
- ACM Fellow. 2010.
- IEEE Fellow. 2004.
- University of Illinois Willett Faculty Scholar, 2002-2009.

Have you previously been involved in any CRA activities? If so, describe.

- Council Member, The Computing Community Consortium (CCC) of CRA, January 2011-June 2014. Worked in CCC’s Visioning Subcommittee. Received proposals for visioning workshops, reviewed them, evaluated and discussed them, and acted as a liaison for one of them.
- Attended the 2015 Leadership in Science Policy Institute Workshop, (LiSPI), CCC, Washington DC, April 2015.
- Co-organizer of two CCC Visioning Workshops on Advancing Computer Architecture Research: "Failure is not an Option: Popular Parallel Programming" (February 2010) and "What Now in ILP Research?” (September 2010). These two workshops lead to the next one below, which in turn influenced the creation of the Exploiting Parallelism and Scalability (XPS) solicitation from NSF. Presented the workshop outcome to CCC, DOE, NSF, AFOSR, and NITRD.
- Co-editor, CCC Visioning white paper: "21st Century Computer Architecture, A Community White Paper", May 2012. Influenced the creation of XPS.
- Participant in the CRA Visioning workshop: "Revitalizing Computer Architecture Research", December 2005.
- Member of the Computing Innovation Fellows Selection Committee, CCC and CRA, 2010.

List any other relevant experience and year(s) it occurred (list--no more than *five* items).

- Director, Illinois-Intel Parallelism Center (I2PC), University of Illinois, September 2011 - September 2013. Center was supported by Intel with $2M. It had 16 faculty. I organized the "2013 Illinois Symposium on Parallelism: Current State of the Field and the Future", Urbana, Sept 2013 (http://i2pc.cs.illinois.edu/parworkshop/2013/schedule.html). I lead the preparation of a book with the research of all the faculty in the Center (http://iacoma.cs.uiuc.edu/iacoma-papers/Illinois_parallelism_book.pdf).
- Director, Center for Programmable Extreme-Scale Computing, Univ. of Illinois, January 2011 - pres. Funded by DARPA, DOE, and NSF to focus on architectures for extreme energy efficiency.
- Professor, Computer Science Department, University of Illinois, August 1992 - pres.

- Leader, University of Illinois OpenSPARC Center of Excellence, September 2007 - August 2010. Center funded by Sun Microsystems. It included 9 faculty.
- Graduated 35 Ph.D. students, 13 of which are now Professors at leading US universities, including Cornell University, University of Washington, Georgia Tech, NCSU, UCSC, University of Rochester, OSU, University of Minnesota, University of Texas San Antonio, Stony Brook University, University of Southern California, and University of Pittsburgh.

Research interests: (list only)
- Computer systems architecture
- Parallel computing
- Computer reliability
- Low power design
- Parallel programming models
- Software debugging

Personal Statement
I've experience serving the computing research community, and hope to continue doing so. I've served for three years in the Computing Community Consortium (CCC) Council, helping shepherd visioning research proposals. I co-organized two workshops on Advancing Computer Architecture Research, which helped lead to the NSF solicitation on Exploiting Parallelism and Scalability (XPS). I've been Chair of IEEE Technical Committee on Computer Architecture (TCCA) for 5 years, where I helped ensure harmonious conference co-operation. At Illinois, I've been the Director of the Intel Center for Parallelism, which grouped 16 faculty. I've graduated 35 PhDs, 13 of which are now faculty.

Brief Biography or CV
http://iacoma.cs.uiuc.edu/iacoma-papers/cv_torrellas_july2015.pdf
(Attached)

Josep Torrellas

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July 2015

Education

Aug 92	Ph.D. in Electrical Engineering, Stanford University. Dissertation: "Multiprocessor Cache Memory Performance: Characterization and Optimization". Advisor: John Hennessy.
Dec 87	M.S. in Electrical and Computer Engineering, University of Wisconsin - Madison.
Jun 86	B.S. in Electrical Engineering, Universitat Politecnica de Catalunya, Spain.

Appointments

Jan 11	-	pres.	Director, Center for Programmable Extreme-Scale Computing, University of Illinois at Urbana-Champaign (UIUC).
Sep 11	-	Sep 13	Director, Illinois-Intel Parallelism Center (I2PC), UIUC.
Aug 02	-	pres.	Professor, Computer Science Department, UIUC.
Aug 02	-	Aug 09	Willett Faculty Scholar, Computer Science Department, UIUC.
Sep 07	-	Aug 10	Leader, University of Illinois OpenSPARC Center of Excellence, UIUC.
Feb 08	-	Aug 11	Computer Architecture Leader, Universal Parallel Computing Research Center (UPCRC), UIUC.
Aug 98	-	Aug 02	Associate Professor, Computer Science Department, UIUC.
May 98	-	Jan 99	Research Staff Member, IBM T.J. Watson Research Center, IBM Research (sabbatical).
Apr 93	-	pres.	Departmental Affiliate, Electrical and Computer Engineering Department, UIUC.
Aug 92	-	Aug 98	Assistant Professor, Computer Science Department, UIUC.
Sep 92	-	Dec 96	Senior Computer Systems Engineer, Center for Supercomp. Research and Develop. (CSRD), UIUC.

Honors & Awards

2015	IEEE Computer Society Technical Achievement Award, June 2015. For "Pioneering contributions to shared-memory multiprocessor architectures and thread-level speculation".
2015	Honorable Mention Paper, IEEE Micro Special Issue: 2015 Micro's Top Picks from Computer Architecture Conferences.
2014	Distinguished Paper Award, International Conference on Programming Language Design and Implementation (PLDI), June 2014.
2014	Best Paper Award Finalist, International Symposium on High Performance Computer Architecture (HPCA), Feburary 2014.
2013	Distinguished Speaker Award, IEEE International Conference on Application Specific Systems, Architectures and Processors (ASAP), June 2013.
2012	High-Impact Paper Award, International Conference on Computer Design (ICCD), October 2012. For "One of the 5 most cited papers in the first 30 years of ICCD (1983-2012)".
2012	Jon Postel Distinguished Lecturer, Computer Science Department, UCLA, November 2012.
2010	ACM Fellow.
2009	Best Paper Award, 42nd International Symposium on Microarchitecture (MICRO), December 2009.
2009	Paper in 2009 IEEE Micro's Top Picks from Computer Architecture Conferences.
2009	Research Highlight paper in Communications of the ACM (CACM).
2009	Best Idea Award, Wild and Crazy Ideas Session, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009.
2007	Paper in 2007 IEEE Micro's Top Picks from Computer Architecture Conferences.
2006	Best Paper Award, 39th International Symposium on Microarchitecture (MICRO), December 2006.

2006	Paper in 2006 IEEE Micro's Top Picks from Computer Architecture Conferences.
2004	Paper in 2004 IEEE Micro's Top Picks from Computer Architecture Conferences.
2004	IEEE Fellow.
2003	Paper in 2003 IEEE Micro's Top Picks from Computer Architecture Conferences.
2002-9	Willett Faculty Scholar, UIUC.
2001	Best Paper Award, Fifth Workshop on Multithreaded Execution, Architecture, and Compilation.
2000	Senior Xerox Award for Outstanding Faculty Research, UIUC.
1997-00	IBM Partnership Award.
1997	C. W. Gear Outstanding Junior Faculty Award, UIUC.
1997	Junior Xerox Award for Outstanding Faculty Research, UIUC.
1995,6,8	Intel Research Council Award.
1994-9	Young Investigator Award, National Science Foundation.
1993-6	Research Initiation Award, National Science Foundation.

Main Professional Society Service

Apr 15	Attended the 2015 Leadership in Science Policy Institute Workshop, Computing Community Consortium (CCC), Washington DC.
Jan 11 - Jun 14	Council Member, The Computing Community Consortium (CCC), Computing Research Association (CRA). Member of the Subcommittee on Visioning Activities.
June 13	Chair and co-editor, "SIGARCH/TCCA's Recommended Best Practices for ISCA Program Chairs".
May 12	Co-editor, CCC Visioning white paper: "21st Century Computer Architecture, A Community White Paper".
Oct 10 - Oct 19	Member of the Executive Committee, The Institute of Electrical and Electronics Engineers (IEEE) Technical Committee on Computer Architecture (TCCA).
Jul 05 - Oct 10	Chair, IEEE TCCA. Main activities included: organize and fund over 10 technical conferences yearly, co-ordinate the funding and publicity of the Computer Architecture Letters, provide funds for students to travel to conferences, serve in the Steering Committees of conferences, and co-locate ACM PPoPP and IEEE HPCA for interdisciplinary interactions.
Feb 10 - Sep 10	Co-organizer of two CCC Visioning Workshops on Advancing Computer Architecture Research: "Failure is not an Option: Popular Parallel Programming" and "What Now in ILP Research?".
Dec 05	Participant in the CRA Visioning workshop: "Revitalizing Computer Architecture Research".
Jul 98 - Jul 05	Vice-Chair and Member of the Advisory Board, IEEE TCCA.

Designed Architectures

1. *QuickRec: A Hardware Prototype for Recording and Deterministically Replaying Multithreaded Programs in the Intel Architecture*. This prototype has been developed in collaboration with Intel, and is described in the QuickRec ISCA-2013 paper: http://iacoma.cs.uiuc.edu/iacoma-papers/isca13_1.pdf.

2. *Runnemede: An Chip Multiprocessor for Extreme-Scale Computing*. This manycore chip has been designed in collaboration with Intel, and is described in the Runnemede HPCA-2013 paper: http://iacoma.cs.uiuc.edu/iacoma-papers/hpca13_1.pdf.

Designed Software

1. *VARIUS and VARIUS-NTV: A Model of Process Variation*. This tool models within-die process variation and the resulting timing errors in manycores at a level suitable for microarchitects. June 2007. http://iacoma.cs.uiuc.edu/varius/index.html.

2. *SESC: A Simulator of Superscalar Multiprocessors and Memory Systems with Thread-Level Speculation Support*. SESC is a multiprocessor simulator package with support for thread-level speculation. June 2005. http://sourceforge.net/projects/sesc.

3. *Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors*. Scal-Tool is a public-domain tool that is available through the NCSA software repository. May 1999.

4. *Augmint: A Multiprocessor Simulation Environment for Intel x86 Architectures*. Augmint is a multiprocessor tracing and evaluation package that runs on Intel x86 machines. December 1995. http://iacoma.cs.uiuc.edu/augmint.html.

Publications. Conferences

1. Tanmay Gangwani, Adam Morrison, and Josep Torrellas, *ParSync: Breaking Serialization in Lock-Free Multicore Synchronization*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2016.

2. Sergi Abadal, Eduard Alarcon, Albert Cabellos, and Josep Torrellas, *WiSync: An Architecture for Fast On-Chip Synchronization through Wireless-Enabled Global Communication*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2016.

3. Yuelu Duan, David Koufaty, and Josep Torrellas, *SCsafe: Logging Sequential Consistency Violations Continuously and Precisely*, International Symposium on High Performance Computer Architecture (HPCA), March 2016.

4. Bhargava Gopireddy, Choungki Song, Josep Torrellas, Nam Sung Kim, Aditya Agrawal, and Asit Mishra, *ScalCore: Designing a Core for Voltage Scalability*, International Symposium on High Performance Computer Architecture (HPCA), March 2016.

5. Yuelu Duan, Nima Honarmand and Josep Torrellas, *Asymmetric Memory Fences: Optimizing Both Performance and Implementability*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2015.

6. Ehsan Totoni, Josep Torrellas, and Laxmikant V. Kale, *Using an Adaptive HPC Runtime System to Reconfigure the Cache Hierarchy*, International Conference for High Performance Computing, Networking, Storage and Analysis (SC), November 2014.

7. Nima Honarmand and Josep Torrellas, *Replay Debugging: Leveraging Record and Replay for Program Debugging*, International Symposium on Computer Architecture (ISCA), June 2014.

8. Xuehai Qian, Benjamin Sahelices, and Josep Torrellas, *OmniOrder: Directory-Based Coherence for Conflict Serialization*, International Symposium on Computer Architecture (ISCA), June 2014.

9. Wonsun Ahn, Jiho Choi, Thomas Shull, Maria Garzaran, and Josep Torrellas, *Improving JavaScript Performance Through Predictable Type Specialization* International Conference on Programming Language Design and Implementation (PLDI), June 2014. **Distinguished Paper Award**.

10. Nima Honarmand and Josep Torrellas, *RelaxReplay: Record and Replay for Relaxed-Consistency Multiprocessors*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2014.

11. Josep Torrellas, *Extreme-Scale Computer Architecture: Energy Efficiency from the Ground Up*, Design Automation and Test in Europe (DATE), March 2014.

12. Aditya Agrawal, Amin Ansari, and Josep Torrellas, *Mosaic: Exploiting the Spatial Locality of Process Variation to Reduce Refresh Energy in On-Chip eDRAM Modules*, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

13. Amin Ansari, Asit Mishra, Jianping Xu, and Josep Torrellas, *Tangle: Route-Oriented Dynamic Voltage Minimization for Variation-Afflicted, Energy-Efficient On-Chip Networks*, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

14. Shanxiang Qi, Abdullah Muzahid, Wonsun Ahn, and Josep Torrellas, *Dynamically Detecting and Tolerating IF-Condition Data Races*, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

15. Xuehai Qian, Benjamin Sahelices, Josep Torrellas, and Depei Qian, *BulkCommit: Scalable and Fast Commit of Atomic Blocks in a Lazy Multiprocessor Environment*, International Symposium on Microarchitecture (MICRO), December 2013.

16. Gilles Pokam, Klaus Danne, Cristiano Pereira, Rolf Kassa, Tim Kranich, Shiliang Hu, and Justin Gottschlich (Intel), and Nima Honarmand, Nathan Dautenhahn, Sam King and Josep Torrellas (UIUC), *QuickRec: Prototyping an Intel Architecture Extension for Record and Replay of Multithreaded Programs*, International Symposium on Computer Architecture (ISCA), June 2013.

17. Yuelu Duan, Abdullah Muzahid, and Josep Torrellas, *WeeFence: Toward Making Fences Free in TSO*, International Symposium on Computer Architecture (ISCA), June 2013.

18. Wonsun Ahn, Yuelu Duan and Josep Torrellas, *DeAliaser: Alias Speculation Using Atomic Region Support*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2013.

19. by Nima Honarmand, Nathan Dautenhahn, Josep Torrellas, Samuel King, Gilles Pokam and Cristiano Pereira, *Cyrus: Unintrusive Application-Level Record-Replay for Replay Parallelism*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2013.

20. Xuehai Qian, Benjamin Sahelices, Josep Torrellas and Depei Qian, *Volition: Scalable and Precise Sequential Consistency Violation Detection*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2013.

21. Nicholas P. Carter, Aditya Agrawal, Shekhar Borkar, Romain Cledat, Howard David, Dave Dunning, Joshua Fryman, Ivan Ganev, Roger A. Golliver, Rob Knauerhase, Richard Lethin, Benoit Meister, Asit K. Mishra, Wilfred R. Pinfold, Justin Teller, Josep Torrellas, Nicolas Vasilache, Ganesh Venkatesh, and Jianping Xu, *Runnemede: An Architecture for Ubiquitous High-Performance Computing*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

22. Ulya R. Karpuzcu, Abhishek Sinkar, Nam Sung Kim, and Josep Torrellas, *EnergySmart: Toward Energy-Efficient Manycores for Near-Threshold Computing*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

23. Aditya Agrawal, Prabhat Jain, Amin Ansari and Josep Torrellas, *Refrint: Intelligent Refresh to Minimize Power in On-Chip Multiprocessor Cache Hierarchies*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

24. Amin Ansari, Shuguang Feng, Shantanu Gupta, Josep Torrellas, and Scott Mahlke, *Illusionist: Transforming Lightweight Cores into Aggressive Cores on Demand*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

25. Abdullah Muzahid, Shanxiang Qi and Josep Torrellas, *Vulcan: Hardware Support for Detecting Sequential Consistency Violations Dynamically*, International Symposium on Microarchitecture (MICRO), December 2012.

26. Josep Torrellas, *FlexRAM: Toward an Advanced Intelligent Memory System. A Retrospective Paper*, International Conference on Computer Design (ICCD), September 2012.

27. Ulya R. Karpuzcu, Krishna B. Kolluru, Nam Sung Kim and Josep Torrellas, *VARIUS-NTV: A Microarchitectural Model to Capture the Increased Sensitivity of Manycores to Process Variations at Near-Threshold Voltages*, International Conference on Dependable Systems and Networks (DSN), June 2012. Acceptance Rate: 17%.

28. Ehsan Totoni, Babak Behzad, Swapnil Ghike and Josep Torrellas, *Comparing the Power and Performance of Intel's SCC to State-of-the-Art CPUs and GPUs*, International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2012.

29. Xuehai Qian, Benjamin Sahelices and Josep Torrellas, *BulkSMT: Designing SMT Processors for Atomic-Block Execution*, International Symposium on High Perfomance Computer Architecture (HPCA), February 2012.

30. Shanxiang Qi, Norimasa Otsuki, Lois Orosa, Abdullah Muzahid, and Josep Torrellas, *Pacman: Tolerating Asymmetric Data Races with Unintrusive Hardware*, International Symposium on High Perfomance Computer Architecture (HPCA), February 2012.

31. Yuelu Duan, Xing Zhou, Wonsun Ahn, and Josep Torrellas, *BulkCompactor: Optimized Deterministic Execution via Conflict-Aware Commit of Atomic Blocks*, International Symposium on High Perfomance Computer Architecture (HPCA), February 2012.

32. Rishi Agarwal and Josep Torrellas, *FlexBulk: Intelligently Forming Atomic Blocks in Blocked-Execution Multiprocessors to Minimize Squashes*, International Symposium on Computer Architecture (ISCA), June 2011.

33. Rishi Agarwal, Pranav Garg, and Josep Torrellas, *Rebound: Scalable Checkpointing for Coherent Shared Memory*, International Symposium on Computer Architecture (ISCA), June 2011.

34. Xuehai Qian, Wonsun Ahn, and Josep Torrellas, *ScalableBulk: Scalable Cache Coherence for Atomic Blocks in a Lazy Environment*, International Symposium on Microarchitecture (MICRO), December 2010. (17% acceptance rate).

35. Abdullah Muzahid, Norimasa Otsuki, and Josep Torrellas, *AtomTracker: A Comprehensive Approach to Atomic Region Inference and Violation Detection*, International Symposium on Microarchitecture (MICRO), December 2010. (17% acceptance rate).

36. Adrian Nistor, Darko Marinov, and Josep Torrellas, *InstantCheck: Checking the Determinism of Parallel Programs Using On-the-fly Incremental Hashing*, International Symposium on Microarchitecture (MICRO), December 2010. (17% acceptance rate).

37. Brian Greskamp, Ulya R. Karpuzcu, and Josep Torrellas, *LeadOut: Composing Low-Overhead Frequency-Enhancing Techniques for Single-Thread Performance in Configurable Multicores*, International Symposium on High-Performance Computer Architecture (HPCA), January 2010.

38. Wonsun Ahn, Shanxiang Qi, Jae-Woo Lee, Marios Nicolaides, Xing Fang, Josep Torrellas, David Wong, and Samuel Midkiff, *BulkCompiler: High-Performance Sequential Consistency through Cooperative Compiler and Hardware Support*, International Symposium on Microarchitecture (MICRO), December 2009.

39. Ulya R. Karpuzcu, Brian Greskamp and Josep Torrellas, *The BubbleWrap Many-Core: Popping Cores for Sequential Acceleration*, International Symposium on Microarchitecture (MICRO), December 2009. **Best Paper Award**.

40. Adrian Nistor, Darko Marinov, and Josep Torrellas, *Light64: Lightweight Hardware Support for Race Detection during Systematic Testing of Parallel Programs*, International Symposium on Microarchitecture (MICRO), December 2009.

41. Abdullah Muzahid, Dario Suarez, Shanxiang Qi, and Josep Torrellas, *SigRace: Signature-Based Data Race Detection*, International Symposium on Computer Architecture (ISCA), June 2009.

42. Pablo Montesinos, Matthew Hicks, Samuel T. King, and Josep Torrellas, *Capo: A Software-Hardware Interface for Practical Deterministic Multiprocessor Replay*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009.

43. Brian Greskamp, R. Ulya Karpuzcu, and Josep Torrellas, *BubbleWrap: Popping CMP Cores for Sequential Acceleration*, Wild and Crazy Ideas Session, at International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009. **Best Idea Award**.

44. Brian Greskamp, Lu Wan, Ulya R. Karpuzcu, Jeffrey J. Cook, Josep Torrellas, Deming Chen, and Craig Zilles, *BlueShift: Designing Processors for Timing Speculation from the Ground Up*, International Symposium on High-Performance Computer Architecture (HPCA), February 2009.

45. Abhishek Tiwari and Josep Torrellas, *Facelift: Hiding and Slowing Down Aging in Multicores*, International Symposium on Microarchitecture (MICRO), November 2008.

46. Smruti Sarangi, Brian Greskamp, Abhishek Tiwari, and Josep Torrellas, *EVAL: Utilizing Processors with Variation-Induced Timing Errors*, International Symposium on Microarchitecture (MICRO), November 2008.

47. Pablo Montesinos, Luis Ceze, and Josep Torrellas, *DeLorean: Recording and Deterministically Replaying Shared-Memory Multiprocessor Execution Efficiently*, International Symposium on Computer Architecture (ISCA), June 2008.

48. Radu Teodorescu and Josep Torrellas, *Variation-Aware Application Scheduling and Power Management for Chip Multiprocessors*, International Symposium on Computer Architecture (ISCA), June 2008.

49. James Tuck, Wonsun Ahn, Luis Ceze, and Josep Torrellas, *SoftSig: Software-Exposed Hardware Signatures for Code Analysis and Optimization*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2008.

50. Karin Strauss, Xiaowei Shen, and Josep Torrellas, *Unconstrained Snoop Request Delivery in Embedded-Ring Multiprocessors*, International Symposium on Microarchitecture (MICRO), December 2007.

51. Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas, *Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing*, International Symposium on Microarchitecture (MICRO), December 2007.

52. James Tuck, Wei Liu, and Josep Torrellas, *CAP: Criticality Analysis for Power-Efficient Speculative Multithreading*, International Conference on Computer Design (ICCD), October 2007.

53. Cyrus Bazeghi, Francisco J. Mesa-Martinez, Brian Greskamp, Josep Torrellas, and Jose Renau, *Estimating Design Time for System Circuits*, International Conference on Very Large Scale Integration (VLSI-SoC), October 2007.

54. Brian Greskamp and Josep Torrellas, *Paceline: Improving Single-Thread Performance in Nanoscale CMPs through Core Overclocking*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2007.

55. Luis Ceze, James M. Tuck, Pablo Montesinos, and Josep Torrellas, *BulkSC: Bulk Enforcement of Sequential Consistency*, International Symposium on Computer Architecture (ISCA), June 2007.

56. Abhishek Tiwari, Smruti Sarangi, and Josep Torrellas, *ReCycle: Pipeline Adaptation to Tolerate Parameter Variation*, International Symposium on Computer Architecture (ISCA), June 2007.

57. Pablo Montesinos, Wei Liu, and Josep Torrellas, *Using Register Lifetime Predictions to Protect Register Files Against Soft Errors*, International Conference on Dependable Systems and Networks (DSN), June 2007.

58. Brian Greskamp, Smruti Sarangi, and Josep Torrellas, *Threshold Voltage Variation Effects on Aging-Related Hard Failure Rates*, International Symposium on Circuits and Systems (ISCAS), Special Session: Circuit Design in the Presence of Device Variability, May 2007.

59. Smruti Sarangi, Brian Greskamp, and Josep Torrellas, *A Model for Timing Errors in Processors with Parameter Variation*, International Symposium on Quality Electronic Design (ISQED), March 2007.

60. Luis Ceze, Pablo Montesinos, Christoph von Praun, and Josep Torrellas, *Colorama: Architectural Support for Data-Centric Synchronization*, International Symposium on High-Performance Computer Architecture (HPCA), February 2007.

61. Smruti R. Sarangi, Abhishek Tiwari, and Josep Torrellas, *Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware*, International Symposium on Microarchitecture (MICRO), December 2006. **Best Paper Award.**

62. James Tuck, Luis Ceze, and Josep Torrellas, *Scalable Cache Miss Handling for High Memory-Level Parallelism*, International Symposium on Microarchitecture (MICRO), December 2006.

63. Shan Lu, Pin Zhou, Wei Liu, Yuanyuan Zhou, and Josep Torrellas, *PathExpander: Architectural Support for Increasing the Path Coverage of Dynamic Bug Detection*, International Symposium on Microarchitecture (MICRO), December 2006.

64. Pablo Montesinos, Wei Liu, and Josep Torrellas, *Shield: Cost-Effective Soft-Error Protection for Register Files*, Third IBM TJ Watson Conference on Interaction between Architecture, Circuits and Compilers (P=AC2), October 2006.

65. L. Ceze, J. Tuck, C. Cascaval, and J. Torrellas, *Bulk Disambiguation of Speculative Threads in Multiprocessors*, International Symposium on Computer Architecture (ISCA), June 2006.

66. K. Strauss, X. Shen, and J. Torrellas, *Flexible Snooping: Adaptive Forwarding and Filtering of Snoops in Embedded-Ring Multiprocessors*, International Symposium on Computer Architecture (ISCA), June 2006.

67. S. Sarangi, B. Greskamp, and J. Torrellas, *CADRE: Cycle-Accurate Deterministic Replay for Hardware Debugging*, International Conference on Dependable Systems and Networks (DSN), June 2006.

68. W. Liu, J. Tuck, L. Ceze, W. Ahn, K. Strauss, J. Renau and J. Torrellas, *POSH: A TLS Compiler that Exploits Program Structure*, Symposium on Principles and Practice of Parallel Programming (PPoPP), March 2006.

69. J. Nakano, P. Montesinos, K. Gharachorloo, and J. Torrellas, *ReViveI/O: Efficient Handling of I/O in Highly-Available Rollback-Recovery Servers*, International Symposium on High-Performance Computer Architecture (HPCA), February 2006.

70. S. Sarangi, W. Liu, J. Torrellas, and Y. Zhou, *ReSlice: Selective Re-Execution of Long-Retired Misspeculated Instructions Using Forward Slicing*, International Symposium on Microarchitecture (MICRO), November 2005.

71. W. Liu, J. Tuck, L. Ceze, K. Strauss, J. Renau, and J. Torrellas, *POSH: A Profiler-Enhanced TLS Compiler that Leverages Program Structure*, Watson Conference on Interaction between Architecture, Circuits, and Compilers (P=AC2), September 2005.

72. M. Wei, M. Snir, J. Torrellas, and R. B. Tremaine, *A Near-Memory Processor for Vector, Streaming and Bit Manipulation Workloads*, Watson Conference on Interaction between Architecture, Circuits, and Compilers (P=AC2), September 2005.

73. J. Renau, K. Strauss, L. Ceze, W. Liu, S. Sarangi, J. Tuck, and J. Torrellas, *Thread-Level Speculation on a CMP Can Be Energy Efficient*, International Conference on Supercomputing (ICS), June 2005.

74. J. Renau, J. Tuck, W. Liu, L. Ceze, K.Strauss, and J. Torrellas, *Tasking with Out-of-Order Spawn in TLS Chip Multiprocessors: Microarchitecture and Compilation*, International Conference on Supercomputing (ICS), June 2005.

75. R. Teodorescu and J. Torrellas, *Prototyping Architectural Support for Program Rollback Using FPGAs*, Symposium on Field-Programmable Custom Computing Machines (FCCM), April 2005.

76. P. Zhou, W. Liu, F. Long, S. Lu, F. Qin, Y. Zhou, S. Midkiff and J. Torrellas, *AccMon: Automatically Detecting Memory-Related Bugs via Program Counter-Based Invariants*, International Symposium on Microarchitecture (MICRO), December 2004.

77. P. Zhou, F. Qin, W. Liu, Y. Zhou, and J. Torrellas, *iWatcher: Efficient Architectural Support for Software Debugging*, International Symposium on Computer Architecture (ISCA), June 2004.

78. A. Nguyen and J. Torrellas, *Design Trade-offs in High-Throughput Coherence Controllers*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2003. Acceptance Rate: 17%.

79. M. Garzaran, M. Prvulovic, J. Llaberia, V. Vinals, L. Rauchwerger, and J. Torrellas, *Using Software Logging to Support Multi-Version Buffering in Thread-Level Speculation*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2003. Acceptance Rate: 17%.

80. B. Fraguela, J. Renau, P. Feautrier, D. Padua, and Josep Torrellas, *Programming the FlexRAM Parallel Intelligent Memory System*, International Symposium on Principles and Practice of Parallel Programming (PPoPP), June 2003.

81. M. Prvulovic and J. Torrellas, *ReEnact: Using Thread-Level Speculation to Debug Data Races in Multithreaded Codes*, International Symposium on Computer Architecture (ISCA), June 2003.

82. M. Huang, J. Renau, and J. Torrellas, *Positional Adaptation of Processors: Application to Energy Reduction*, International Symposium on Computer Architecture (ISCA), June 2003.

83. M. Garzaran, M. Prvulovic, J. Llaberia, V. Vinals, L. Rauchwerger, and J. Torrellas, *Tradeoffs in Buffering Memory State for Thread-Level Speculation in Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 2003.

84. J. Martinez, J. Renau, M. Huang, M. Prvulovic, and J. Torrellas, *Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors*, International Symposium on Microarchitecture (MICRO), November 2002.

85. J. Martinez and J. Torrellas, *Speculative Synchronization: Applying Thread-Level Speculation to Parallel Applications*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), October 2002. Acceptance Rate: 18%.

86. M. Huang, J. Renau, and J. Torrellas, *Energy-Efficient Hybrid Wakeup Logic*, International Symposium on Low Power Electronics and Design (ISLPED), August 2002. Acceptance Rate: 24%.

87. M. Prvulovic, Z. Zhang, and J. Torrellas. *ReVive: Cost-Effective Architectural Support for Rollback Recovery in Shared-Memory Multiprocessors*, International Symposium on Computer Architecture (ISCA), May 2002. Acceptance Rate: 15%.

88. Y. Solihin, J. Lee, and J. Torrellas, *Using a User-Level Memory Thread for Correlation Prefetching*, International Symposium on Computer Architecture (ISCA), May 2002. Acceptance Rate: 15%.

89. M. Cintra and J. Torrellas, *Eliminating Squashes Through Learning Cross-Thread Violations in Speculative Parallelization for Multiprocessors*, Eigth International Symposium on High-Performance Computer Architecture (HPCA), February 2002.

90. M. Garzaran, M. Prvulovic, A. Jula, H. Yu, Y. Zhang, L. Rauchwerger, and J. Torrellas, *Architectural Support for Parallel Reductions in Scalable Shared-Memory Multiprocessors*, International Conference on Parallel Architectures and Compilation Techniques (PACT), Barcelona, September 2001.

91. M. Huang, J. Renau, S.-M. Yoo, and J. Torrellas, *L1 Data Cache Decomposition for Energy Efficiency*, International Symposium on Low Power Electronics and Design (ISLPED), pp. 10-15, August 2001. Acceptance Rate: 24%.

92. M. Prvulovic, M. J. Garzaran, L. Rauchwerger, and J. Torrellas. *Removing Architectural Bottlenecks to the Scalability of Speculative Parallelization*, International Symposium on Computer Architecture (ISCA), pp. 204-215, June 2001. Acceptance Rate: 14%.

93. J. Lee, Y. Solihin, and J. Torrellas, *Automatically Mapping Code on an Intelligent Memory Architecture*, International Symposium on High-Performance Computer Architecture (HPCA), pp 121-132, January 2001. Acceptance Rate: 23%.

94. M. Huang, J. Renau, S.-M. Yoo, and J. Torrellas, *A Framework for Dynamic Energy Efficiency and Temperature Management*, International Symposium on Microarchitecture (MICRO), pp 202-213, December 2000. Acceptance Rate: 28%.

95. Q. Cao, J. Torrellas, and H.-V. Jagadish, *Unified Fine-Granularity Buffering of Index and Data: Approach and Implementation*, International Conference on Computer Design (ICCD), September 2000.

96. M. Cintra, J. Martinez and J. Torrellas, *Architectural Support for Scalable Speculative Parallelization in Shared-Memory Multiprocessors*, International Symposium on Computer Architecture (ISCA), pp 13-24, June 2000. Acceptance Rate: 17%.

97. J. Torrellas, L. Yang and A. Nguyen, *Toward a Cost-Effective DSM Organization that Exploits Processor-Memory Integration*, International Symposium on High-Performance Computer Architecture (HPCA), pp. 15-25, January 2000. Acceptance Rate: 21%.

98. Y. Kang, M. Huang, S.-M. Yoo, Z. Ge, D. Keen, V. Lam, P. Pattnaik and J. Torrellas. *FlexRAM: An Advanced Intelligent Memory System*, International Conference on Computer Design (ICCD), 192-201, October 1999. Acceptance Rate: 32%.

99. Q. Cao, P. Trancoso, J.-L. Larriba-Pey, J. Torrellas, R. Knighten and Y. Won. *Detailed Characterization of a Quad Pentium Pro Server Running TPC-D*, International Conference on Computer Design (ICCD), pp 108-115, October 1999. Acceptance Rate: 32%.

100. P. Trancoso and J. Torrellas. *Cache Optimization for Memory-Resident Decision Support Commercial Workloads*, International Conference on Computer Design (ICCD), pp 546-554, October 1999. Acceptance Rate: 32%.

101. Y. Solihin, V. Lam, and J. Torrellas, *Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors*, Supercomputing 99, November 1999.

102. V. Krishnan and J. Torrellas, *The Need for Fast Communication in Hardware-Based Speculative Chip Multiprocessors*, International Conference on Parallel Architectures and Compilation Techniques (PACT), October 1999.

103. A. Ramirez, J.-L. Larriba-Pey, C. Navarro, X. Serrano, J. Torrellas, and M. Valero. *Optimization of Instruction Fetch for Decision Support Workloads*, International Conference on Parallel Processing (ICPP), September 1999. Acceptance Rate: 32%.

104. D. Koufaty and J. Torrellas. *Compiler Support for Data Forwarding in Scalable Shared-Memory Multiprocessors*, International Conference on Parallel Processing (ICPP), September 1999. Acceptance Rate: 32%.

105. J. Martinez, J. Torrellas, and J. Duato. *Improving the Performance of Bristled CC-NUMA Systems Using Virtual Channels and Adaptivity*, International Conference on Supercomputing (ICS), June 1999.

106. A. Ramirez, J.-L. Larriba-Pey, C. Navarro, J. Torrellas, and M. Valero. *Software Trace Cache*, International Conference on Supercomputing (ICS), June 1999. Acceptance Rate: 31%.

107. Y. Zhang, L. Rauchwerger and J. Torrellas. *Hardware for Speculative Parallelization of Partially-Parallel Loops in DSM Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), January 1999. Acceptance Rate: 31%.

108. J.Torrellas. *Upcoming Architectural Advances in DSM Machines and Their Impact on Programmability*, SIAM Conference on Parallel Processing for Scientific Computing, March 1999.

109. V. Krishnan and J. Torrellas. *A Direct-Execution Framework for Fast and Accurate Simulation of Superscalar Processors*, in International Conference on Parallel Architectures and Compilation Techniques (PACT), October 1998.

110. Y. Kang, J. Torrellas, and T. Huang. *An IRAM Architecture for Image Analysis and Pattern Recognition*, in International Conference on Pattern Recognition, 1998.

111. V. Krishnan and J. Torrellas. *Hardware and Software Support for Speculative Execution of Sequential Binaries on a Chip-Multiprocessor*, in International Conference on Supercomputing (ICS), July 1998.

112. D. Koufaty and J. Torrellas. *Comparing Data Forwarding and Data Prefetching for Communication-Induced Misses in Shared-Memory MPs*, in International Conference on Supercomputing (ICS), July 1998.

113. V. Krishnan and J. Torrellas. *A Clustered Approach to Multithreaded Processors*, in International Parallel Processing Symposium (IPPS), March 1998.

114. Y. Zhang, L. Rauchwerger, and J. Torrellas. *Hardware for Speculative Run-Time Parallelization in Distributed Shared-Memory Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 1998. Acceptance Rate: 22%.

115. S. Basu and J. Torrellas. *Enhancing Memory Use in Simple Coma: Multiplexed Simple Coma*, International Symposium on High-Performance Computer Architecture (HPCA), February 1998. Acceptance Rate: 22%.

116. P. Trancoso, J. Larriba, Z. Zhang and J. Torrellas. *The Memory Performance of DSS Commercial Workloads in Shared-Memory Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 1997. Acceptance Rate: 20%.

117. Z. Zhang and J. Torrellas. *Reducing Remote Conflict Misses: NUMA with Remote Cache versus COMA*, International Symposium on High-Performance Computer Architecture (HPCA), February 1997. Acceptance Rate: 20%.

118. L. Yang and J. Torrellas. *Speeding up the Memory Hierarchy in Flat COMA Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 1997. Acceptance Rate: 20%.

119. J. Torrellas and D. Padua. *The Illinois Aggressive Coma Multiprocessor Project (I-ACOMA)*, Frontiers of Massively Parallel Computation Symposium, October 1996.

120. M. P. Malumbres, J. Duato and J. Torrellas. *An Efficient Implementation of Tree-Based Multicast Routing in Wormhole Networks*, International Symposium on Parallel and Distributed Processing (ISPDP), October 1996.

121. A. Nguyen, M. Michael, A. Sharma, and J. Torrellas. *The Augmint Multiprocessor Simulation Toolkit for Intel x86 Architectures*, International Conference on Computer Design (ICCD), October 1996.

122. P. Trancoso and J. Torrellas. *The Impact of Speeding up Critical Sections with Data Prefetching and Forwarding*, International Conference on Parallel Processing (ICPP), August 1996. Acceptance Rate: 33%.

123. C. Xia and J. Torrellas. *Instruction Prefetching of Systems Codes With Layout Optimized for Reduced Cache Misses*, International Symposium on Computer Architecture (ISCA), June 1996. Acceptance Rate: 25%.

124. L. Yang and J. Torrellas. *Optimizing Primary Data Caches for Parallel Scientific Applications: The Pool Buffer Approach*, International Conference on Supercomputing (ICS), June 1996.

125. A.Raynaud, Z.Zhang, and J.Torrellas. *Distance-Adaptive Update Protocols for Scalable Shared-Memory Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), January 1996. Acceptance Rate: 22%.

126. C. Xia and J.Torrellas. *Improving the Data Cache Performance of Multiprocessor Operating Systems*, International Symposium on High-Performance Computer Architecture (HPCA), January 1996. Acceptance Rate: 22%.

127. D. Koufaty, X. Chen, D. Poulsen, and J. Torrellas. *Data Forwarding in Scalable Shared-Memory Multiprocessors*, International Conference on Supercomputing (ICS), July 1995.

128. Z.Zhang and J.Torrellas. *Speeding up Irregular Applications in Shared-Memory Multiprocessors: Memory Binding and Group Prefetching*, International Symposium on Computer Architecture (ISCA), June 1995. Acceptance Rate: 20%.

129. J.Torrellas, C.Xia, and R.Daigle. *Optimizing Instruction Cache Performance for Operating System Intensive Workloads*, International Symposium on High-Performance Computer Architecture (HPCA), January 1995. Acceptance Rate: 18%.

130. J.Torrellas. *Scalable Shared-Memory Architectures*, 28th Hawaii International Conference on System Sciences (HICSS), January 1995.

131. J.Torrellas and Z.Zhang. *The Performance of the Cedar Multistage Switching Network*, Supercomputing '94, November 1994.

132. D.K.Chen, J.Torrellas and P.C.Yew. *An Efficient Algorithm for the Run-Time Parallelization of Do-Across Loops*, Supercomputing '94, November 1994.

133. J.Torrellas, D.Koufaty, and D.Padua. *Comparing the Performance of the DASH and Cedar Multiprocessors for Scientific Applications*, International Conference on Parallel Processing (ICPP), August 1994.

134. J.Torrellas, A.Tucker, and A.Gupta. *Benefits of Cache-Affinity Scheduling in Shared-Memory Multiprocessors: A Summary*, 1993 ACM Sigmetrics Conference, May 1993. Acceptance Rate: 25%.

135. J.Torrellas, A.Gupta, and J.Hennessy. *Characterizing the Caching and Synchronization Performance of a Multiprocessor Operating System*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), October 1992. Acceptance Rate: 16%.

136. J.Torrellas and J.Hennessy. *Estimating the Performance Advantages of Relaxing Consistency in a Shared-Memory Multiprocessor*, International Conference on Parallel Processing (ICPP), August 1990.

137. J.Torrellas, M.Lam, and J.Hennessy. *Shared Data Placement Optimizations to Reduce Multiprocessor Cache Miss Rates*, International Conference on Parallel Processing (ICPP), August 1990. Acceptance Rate: 29%.

138. J.Torrellas, J.Hennessy, and T.Weil. *Analysis of Critical Architectural and Program Parameters in a Hierarchical Shared-Memory Multiprocessor*, Sigmetrics Conference, May 1990. Acceptance Rate: 22%.

Publications. Books

1. Josep Torrellas, Sarita V. Adve, Vikram S. Adve, Danny Dig, Minh N. Do, Maria Jesus Garzaran, John C. Hart, Thomas S. Huang, Wen-mei W. Hwu, Samuel T. King, Darko Marinov, Klara Nahrstedt, David A. Padua, Madhusudan Parthasarathy, Sanjay J. Patel, and Marc Snir, *Making Parallel Programming Easy: Research Contributions from Illinois*, September 2013.

2. Smruti R. Sarangi and Josep Torrellas, *Techniques to Mitigate the Effects of Congenital Faults in Processors*, 160 pages, ISBN: 978-3-639-04637-3, VDM Verlag, 2008.

3. H. Hadimiouglu, D. Kaeli, J. Kuskin, A. Nanda, J. Torrellas, editors, *High Performance Memory Systems*, 290 pages, ISBN: 0-387-00310-X, Springer-Verlag, New York, 2003.

Publications. Chapters in Books

1. J. Torrellas, *Micro-Architecture Challenges and Energy Management at Near-Threshold Computing*, Near Threshold Computing - Technology, Methods and Applications, Michael Huebner and Cristina Silvano Editors, Springer, 2015.

2. J. Torrellas, *Thread-Level Speculation*, Encyclopedia of Parallel Computing, Springer Science+Business Media LLC, 2011.

3. J. Torrellas, *Cache-Only Memory Architecture*, Encyclopedia of Parallel Computing, Springer Science+Business Media LLC, 2011.

4. P. Trancoso and J. Torrellas, *Exploiting Intelligent Memory for Database Workloads*, in High Performance Memory Systems, Springer-Verlag, 2003.

5. M. Garzaran, M. Prvulovic, J. Llaberia, V. Vinals, L. Rauchwerger, and J. Torrellas, *Software Logging under Speculative Parallelization*, in High Performance Memory Systems, Springer-Verlag, 2003.

6. J. Martinez and J. Torrellas, *Speculative Locks for Concurrent Execution of Critical Sections in Shared-Memory Multiprocessors*, in High Performance Memory Systems, Springer-Verlag, 2003.

7. M. Huang, J. Renau, S. Yoo, and J. Torrellas. *Energy/Performance Design of Memory Hierarchies for Processor-in-Memory Chips*, in Lecture Notes in Computer Science (Vol. 2107), Springer-Verlag, 2001.

8. Y. Solihin, J. Lee, and J. Torrellas. *Adaptively Mapping Code on an Intelligent Memory Architecture*, in Lecture Notes in Computer Science (Vol. 2107),Springer-Verlag, 2001.

Publications. Journals

1. J. Torrellas, *Extreme-Scale Computer Architecture: Energy Efficiency from the Ground Up*, National Science Review, Special Issue on High Performance Computing, Oxford University Press, 2015.

2. Ulya Karpuzcu, Nam Sung Kim, and Josep Torrellas, *Coping with Parametric Variation at Near-Threshold Voltages*, IEEE Micro Magazine, Special Issue on Reliability-Aware Microarchitecture Design, Volume:33 Issue:4, July-Aug. 2013.

3. Josep Torrellas, Luis Ceze, James Tuck, Calin Cascaval, Pablo Montesinos, Wonsun Ahn, and Milos Prvulovic, *The Bulk Multicore Architecture for Improved Programmability*, Communications of the ACM (CACM), December 2009.

4. Gilles Pokam, Cristiano Pereira, Klaus Danne, Lynda Yang, Samuel King, and Josep Torrellas, *Hardware and Software Approaches for Deterministic Multiprocessor Replay of Concurrent Programs*, Intel Technology Journal, Issue on Addressing the Challenges of Tera-Scale Computing, Vol. 13, Issue 4, December 2009.

5. Josep Torrellas, *Architectures for Extreme-Scale Computing*, IEEE Computer, November 2009.

6. Derek R. Hower, Pablo Montesinos, Luis Ceze, Mark D. Hill, and Josep Torrellas, *Two Hardware-based Approaches for Deterministic Multiprocessor Replay*, **Research Highlight**, Communications of the ACM (CACM), June 2009.

7. James Tuck, Wonsun Ahn, Luis Ceze, and Josep Torrellas, *SoftSig: Software-Exposed Hardware Signatures for Code Analysis and Optimization*, IEEE Micro Special Issue: **Micro's Top Picks from Computer Architecture Conferences**, January-February 2009.

8. Smruti R. Sarangi, Brian Greskamp, Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas, *VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects*, IEEE Transactions on Semiconductor Manufacturing (IEEE TSM), February 2008.

9. Smruti Sarangi, Satish Narayanasamy, Bruce Carneal, Abhishek Tiwari, Brad Calder, and Josep Torrellas, *Patching Processor Design Errors with Programmable Hardware*, IEEE Micro Special Issue: **Micro's Top Picks from Computer Architecture Conferences**, January-February 2007.

10. L. Ceze, K. Strauss, J. Tuck, J. Renau, and J. Torrellas, *CAVA: Using Checkpoint-Assisted Value Prediction to Hide L2 Misses*, ACM Transactions on Architecture and Code Optimization (TACO), June 2006.

11. R. Teodorescu, J. Nakano, and J. Torrellas, *SWICH: A Prototype for Efficient Cache-Level Checkpointing and Rollback*, IEEE Micro Magazine, IEEE, Inc., vol. 26, September-October, 2006.

12. J. Renau, K. Strauss, L. Ceze, W. Liu, S. Sarangi, J. Tuck, and J. Torrellas, *Energy-Efficient Thread-Level Speculation on a CMP*, IEEE Micro Magazine, Special Issue: 2005 **Micro's Top Picks** from Computer Architecture Conferences, IEEE, Inc., January-February 2006.

13. Josep Torrellas, *Guest Editor's Introduction*, IEEE Micro Magazine, Special Issue: 2005 Micro's Top Picks from Computer Architecture Conferences, IEEE, Inc., January-February 2006.

14. M. J. Garzaran, M. Prvulovic, J. M. Llaberia, V. Vinals, L. Rauchwerger, and J. Torrellas, *Tradeoffs in Buffering Speculative Memory State for Thread-Level Speculation in Multiprocessors*, ACM Transactions on Architecture and Code Optimization (TACO), ACM, Inc., Vol. 2, Num. 3, September 2005.

15. P. Zhou, F. Qin, W. Liu, Y. Zhou, and J. Torrellas, *iWatcher: Simple and General Architectural Support for Software Debugging*, IEEE Micro Special Issue: 2004 **Micro's Top Picks** from Computer Architecture Conferences, November-December 2004.

16. L. Ceze, K. Strauss, J. Tuck, J. Renau and J. Torrellas, *CAVA: Hiding L2 Misses with Checkpoint-Assisted Value Prediction*, IEEE Computer Architecture Letters (CAL), IEEE, Inc., December 2004.

17. Y. Zhou, P. Zhou, F. Qin, W. Liu, and J. Torrellas, *Efficient and Flexible Architectural Support for Dynamic Monitoring*, ACM Transactions on Architecture and Code Optimization (TACO), ACM, Inc., December 2004.

18. J. Martinez and J. Torrellas, *Speculative Synchronization*, IEEE Micro Special Issue: 2003 **Micro's Top Picks** from Computer Architecture Conferences, November-December 2003.

19. M. Huang, J. Renau and J. Torrellas, *Managing Multiple Low-Power Adaptation Techniques: The Positional Approach*, Sidebar, Special Issue on Power-Aware Computing, IEEE Computer, December 2003.

20. Y. Solihin, J. Lee, and J. Torrellas, *Correlation Prefetching with a User-Level Memory Thread*, IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE, Inc., June 2003.

21. A. Ramirez, J.-L. Larriba-Pey, C. Navarro, J. Torrellas, and M. Valero. *Software Trace Cache for Commercial Applications*, International Journal of Parallel Processing (IJPP), Vol. 30, Number 5, October 2002.

22. M. Huang, J. Renau, S.-M. Yoo, and J. Torrellas, *The Design of DEETM: A Framework for Dynamic Energy Efficiency and Temperature Management*, Journal of Instruction-Level Parallelism (JILP), Vol. 3, October 2001.

23. Y. Solihin, J. Lee, and J. Torrellas, *Automatic Code Mapping on an Intelligent Memory Architecture*, Special Issue on High Performance Memory Systems, IEEE Transactions on Computers (TC), IEEE, Inc., Vol. 50, Number 11, November 2001.

24. V. Krishnan and J. Torrellas. *The Need for Fast Communication in Hardware-Based Speculative Chip Multiprocessors*, International Journal of Parallel Processing (IJPP), Vol. 29, Number 1, pp. 3-33, February 2001.

25. V. Krishnan and J. Torrellas. *A Chip Multiprocessor Architecture with Speculative Multithreading*, Special issue on Multithreaded Architecture, IEEE Transactions on Computers (TC), IEEE, Inc., Vol. 48, Number 9, pp. 866-880, September 1999.

26. F. Dahlgren and J. Torrellas. *Cache-Only Memory Architectures*, in IEEE Computer magazine, pp. 72-79, June 1999.

27. C. Xia and J. Torrellas. *Comprehensive Hardware and Software Support for Operating Systems to Exploit MP Memory Hierarchies*, IEEE Transactions on Computers (TC), IEEE, Inc., Vol. 48, Number 5, pp. 494-505, May 1999.

28. Z. Zhang, M. Cintra and J. Torrellas. *Excel-NUMA: Toward Programmability, Simplicity, and High Performance*, Special issue on Cache Memories, IEEE Transactions on Computers (TC), IEEE, Inc., Vol. 48, Number 2, pp. 256-264, February 1999.

29. J. Torrellas, C. Xia, and R. Daigle. *Optimizing Instruction Cache Performance for Operating System Intensive Workloads*, IEEE Transactions on Computers (TC), IEEE, Inc., Vol. 47, Number 12, pp. 1363-1381, December 1998.

30. J.Torrellas and Z.Zhang. *The Performance of the Cedar Multistage Switching Network*, IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE, Inc., Vol. 8, Number 4, pp. 321-336, April 1997.

31. D. Koufaty, X. Chen, D. Poulsen, and J. Torrellas. *Data Forwarding in Scalable Shared-Memory Multiprocessors*, IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE, Inc., Vol. 7, Number 12, pp. 1250-1264, December 1996.

32. J.Torrellas, A.Tucker, and A.Gupta. *Evaluating the Performance of Cache-Affinity Scheduling in Shared-Memory Multiprocessors*, Journal of Parallel and Distributed Computing (JPDC), Academic Press, Inc., Vol. 24, Number 2, pp. 139-151, February 1995.

33. J. Torrellas, M.Lam, and J.Hennessy. *False Sharing and Spatial Locality in Multiprocessor Caches*, IEEE Transactions on Computers (TC), IEEE, Inc., Vol. 43, Number 6, pp. 651-663, June 1994.

Publications. Workshops and Other

1. Mark Hill, Sarita Adve, Luis Ceze, Mary-Jane Irwin, David Kaeli, Margaret Martonosi, Josep Torrellas, Thomas Wenisch, David Wood and Katherine Yelick, *21st Century Computer Architecture*, A Community White Paper, Computing Community Consortium, May 2012.

2. J.Torrellas, M.Oskin, and others, *Failure is not an Option: Popular Parallel Programming*, Report from the CCC-Sponsored First Workshop on Advancing Computer Architecture Research (ACAR-1), October 2010.

3. M.Oskin, J.Torrellas, and others, *Laying a New Foundation for IT: Computer Architecture for 2025 and Beyond*, Report from the CCC-Sponsored Second Workshop on Advancing Computer Architecture Research (ACAR-2), December 2010.

4. Pablo Montesinos, Matthew Hicks, Wonsun Ahn, Samuel T. King, and Josep Torrellas, *Lessons Learned During the Development of the CapoOne Deterministic Multiprocessor Replay System*, Workshop on the Interaction between Operating Systems and Computer Architecture (WIOSCA), June 2009

5. Luis Ceze, Christoph von Praun, Calin Cascaval, Pablo Montesinos, and Josep Torrellas, *Programming and Debugging Shared Memory Programs with Data Coloring*, Workshop on Compilers for Parallel Computing (CPC), January 2009.

6. Abhishek Tiwari and Josep Torrellas, *An Updated Evaluation of ReCycle*, Workshop on Duplicating, Deconstructing, and Debunking (WDDD), June 2008.

7. Luis Ceze, Christoph von Praun, Calin Cascaval, Pablo Montesinos, and Josep Torrellas, *Concurrency Control with Data Coloring*, Workshop on Memory Systems Performance and Correctness (MSPC), March 2008.

8. Ishwar Parulkar, Alan Wood, James C. Hoe, Babak Falsafi, Sarita Adve, Josep Torrellas, and Subhasish Mitra, *OpenSPARC: An Open Platform for Hardware Reliability Experimentation*, Workshop on Silicon Errors in Logic - System Effects (SELSE), March 2008.

9. Radu Teodorescu, Brian Greskamp, Jun Nakano, Smruti R. Sarangi, Abhishek Tiwari and Josep Torrellas, *VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects*, Workshop on Architectural Support for Gigascale Integration (ASGI), June 2007.

10. P. Sack, B. Bliss, Z. Ma, P. Petersen, and J. Torrellas, *Accurate and Efficient Filtering for the Intel Thread Checker Race Detector*, Workshop on Architectural and System Support for Improving Software Dependability (ASID), October 2006.

11. B. Greskamp, S. Sarangi, and J. Torrellas, *Designing Hardware that Supports Cycle-Accurate Deterministic Replay*, Workshop on Complexity-Effective Design (WCED), June 2006.

12. S. Sarangi, B. Greskamp, and J. Torrellas, *Rapid Prototyping in Architecture Research Using Hardware Hooks in COTS Systems*, Workshop on Architectural Research Prototyping (WARP), June 2006.

13. L. Ceze, J. Tuck, and J. Torrellas, *Are We Ready for High Memory-Level Parallelism?*, Workshop on Memory Performance Issues (WMPI), February 2006.

14. C. Bazeghi, F. J. Mesa-Martinez, B. Greskamp, J. Torrellas, and J. Renau, *uComplexity: Estimating Processor Design Effort*, Technical Report UIUCDCS-R-2005-2644, Dept. of Computer Science, UIUC, August 2005.

15. R. Teodorescu and J. Torrellas, *The Design Complexity of Program Undo Support in a General-Purpose Processor*, Workshop on Complexity-Effective Design (WCED), in conjunction with ISCA, June 2005.

16. R. Teodorescu and J. Torrellas, *Empowering Software Debugging Through Architectural Support for Program Rollback*, Workshop on the Evaluation of Software Defect Detection Tools (BUGS), in conjunction with PLDI, June 2005.

17. Y. Zhou and J. Torrellas, *Deploying Architectural Support for Software Defect Detection in Future Processors*, Workshop on the Evaluation of Software Defect Detection Tools (BUGS), in conjunction with PLDI, June 2005.

18. R. Teodorescu and J. Torrellas, *Prototyping Architectural Support for Program Rollback: An Application to Software Debugging*, Workshop on Architecture Research using FPGA Platforms, in conjunction with HPCA-11, February 2005.

19. M. Wei, M. Snir, J. Torrellas, and R. B. Tremaine, *A Brief Description of the NMP ISA and Benchmarks*, Technical Report UIUCDCS-R-2005-2633, Dept. of Computer Science, UIUC, February 2005.

20. B. Fraguela, J. Renau, P. Feautrier, D. Padua, and J. Torrellas. *CFlex: A Programming Language for the FlexRAM Intelligent Memory Architecture*, Technical Report UIUCDCS-R-2002-2287, Dept. of Computer Science, UIUC, July 2002.

21. F. Dang, M. Garzaran, M. Prvulovic, Y. Zhang, A. Jula, H. Yu, N. Amato, L. Rauchwerger, and J. Torrellas, *SmartApps, an Application Centric Approach to High Performance Computing: Compiler-Assisted Software and Hardware Support for Reduction Operations*, NSF Workshop on Next Generation Systems, April 2002.

22. Y. Solihin, J. Lee, and J. Torrellas, *Prefetching in an Intelligent Memory Architecture Using a Helper Thread*, Fifth Workshop on Multithreaded Execution, Architecture, and Compilation, December 2001, (**Best Paper Award**).

23. M. Huang, J. Renau, and J. Torrellas, *Profile-Based Energy Reduction for High-Performance Processors*, Fourth Workshop on Feedback Directed and Dynamic Optimization (FDDO), December 2001.

24. J. Martinez and J. Torrellas, *Speculative Synchronization in Shared-Memory Multiprocessors*, Technical Report UIUCDCS-R-2001-2255, Dept. of Computer Science, UIUC, November 2001.

25. P. Trancoso and J. Torrellas, *Exploiting Intelligent Memory for Database Workloads*, Workshop on Memory Performance Issues, June 2001.

26. M. Garzaran, M. Prvulovic, J. Llaberia, V. Vinals, L. Rauchwerger, and J. Torrellas, *Software Logging under Speculative Parallelization*, Workshop on Memory Performance Issues, June 2001.

27. J. Martinez and J. Torrellas, *Speculative Locks for Concurrent Execution of Critical Sections in Shared-Memory Multiprocessors*, Workshop on Memory Performance Issues, June 2001.

28. J. Martinez and J. Torrellas, *Speculating Past Locks*, UIUC DCS-R-2001-2202 Technical Report, February 2001.

29. Y. Solihin, J. Lee, and J. Torrellas, *Adaptively Mapping Code on an Intelligent Memory Architecture*, 2nd Workshop on Intelligent Memory Systems, November 2000. Acceptance Rate: 27%.

30. M. Huang, J. Renau, S. Yoo, and J. Torrellas, *Energy/Performance Design of Memory Hierarchies for Processor-in-Memory Chips*, 2nd Workshop on Intelligent Memory Systems, November 2000.

31. S.-M. Yoo, J. Renau, M. Huang, and J. Torrellas, *FlexRAM Architecture Design Parameters*, CSRD Technical Report 1584, October 2000.

32. L. Rauchwerger, N. Amato, and J. Torrellas, *SmartApps: An Application-Centric Approach to High Performance Computing*, International Workshop on Languages and Compilers for Parallel Computing (LCPC), August 2000.

33. Y. Solihin, V. Lam and J. Torrellas. *Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors*, Technical Report 1563, Center for Supercomputing Research and Development, May 1999.

34. Y. Zhang, L. Rauchwerger and J. Torrellas. *Hardware for Speculative Reduction Parallelization and Optimization in DSM Multiprocessors*, Workshop on Parallel Computing for Irregular Applications, January 1999.

35. Y. Zhang, L. Rauchwerger and J. Torrellas. *Hardware for Speculative Parallelization in High-End Multiprocessors*, The Third PetaFlop Workshop (TPF-3), February 1999.

36. J. Torrellas. *Computer Architecture Education at the University of Illinois*, IEEE Computer Architecture Technical Committee Newsletter, February 1999.

37. Y. Zhang, L. Rauchwerger, and J. Torrellas. *Hardware for Speculative Reduction Parallelization and Optimization in DSM Multiprocessors*, CSRD Technical Report 1557, December 1998.

38. Y. Zhang, L. Rauchwerger, and J. Torrellas. *A Unified Approach to Speculative Parallelization of Loops in DSM Multiprocessors*, CSRD Technical Report 1542, October 1998.

39. Y.Kang, Z.Ge, M.Huang, D.Keen, V.Lam, S.Yoo, P.Pattnaik and J.Torrellas. *Application-Driven Design of Advanced Intelligent Memory*, CSRD Technical Report, October 1998.

40. P. Trancoso and J. Torrellas. *Cache Optimization for Memory-Resident Decision Support Commercial Workloads*, Technical Report 1538, Center for Supercomputing Research and Development, June 1998.

41. V. Krishnan and J. Torrellas. *Executing Sequential Binaries on a Multithreaded Architecture with Speculation Support*, in Workshop on Multi-Threaded Execution, Architecture and Compilation (MTEAC'98), January 1998.

42. Y. Zhang, L. Rauchwerger, and J. Torrellas. *Hardware for Speculative Run-Time Parallelization in Distributed Shared-Memory Multiprocessors*, CSRD Technical Report 1523, July 1997.

43. L. Yang, A. Nguyen and J. Torrellas. *How Processor-Memory Integration Affects the Design of DSMs*, First Workshop on Mixing Logic and DRAM: Chips that Compute and Remember, June 1997.

44. V. Krishnan and J. Torrellas. *Efficient Use of Processing Transistors for Larger On-Chip Storage: Multithreading*, First Workshop on Mixing Logic and DRAM: Chips that Compute and Remember, June 1997.

45. Z. Zhang, M. Cintra, and J. Torrellas. *Excel-NUMA: Toward Programmability, Simplicity, and High Performance*, CSRD Technical Report 1544, November 1996.

46. J. Torrellas. *Computer Architecture Education at the University of Illinois: Current Status and Some Thoughts*, IEEE Computer Architecture Technical Committee Newsletter, pp. 36-38, June 1996.

47. A. Sharma, A. Nguyen, M. Michael, J. Carbajal, and J. Torrellas. *Augmint: A Multiprocessor Simulation Environment for Intel x86 Architectures*, CSRD Technical Report 1463, December 1995.

48. J.Torrellas, A.Tucker, and A.Gupta. *Evaluating the Benefits of Cache-Affinity Scheduling in Shared-Memory Multiprocessors*, technical report CSL-TR-92-536, Stanford Univ., August 1992.

49. J.Torrellas. *Multiprocessor Cache Memory Performance: Characterization and Optimization*, technical report CSL-TR-92-545, Stanford Univ., August 1992.

50. J.Torrellas, A.Gupta, and J.Hennessy. *Characterizing the Cache Performance and Synchronization Behavior of a Multiprocessor Operating System*, technical report CSL-TR-92-512, Stanford Univ., January 1992.

51. J.Torrellas, M.Lam, and J.Hennessy. *Measurement, Analysis, and Improvement of the Cache Behavior of Shared Data in Cache Coherent Multiprocessors*, technical report CSL-TR-90-412, Stanford Univ., February 1990.

52. J.Torrellas and J.Hennessy. *Estimating the Performance Advantages of Relaxing Consistency in a Shared-Memory Multiprocessor*, technical report CSL-TN-90-365, Stanford Univ., February 1990.

53. J.Torrellas, J.Hennessy, and T.Weil. *A Methodology for Modeling Interprocessor Traffic in Shared-Memory Multiprocessors*, technical report CSL-TR-89-385, Stanford Univ., July 1989.

54. J.Torrellas, B.Bray, K.Cuderman, S.Goldschmidt, A.Kobrin, and A.Zimmerman. *Introductory User's Guide to the Architect's Workbench Tools*, technical report CSL-TR-88-355, Stanford Univ., May 1988.

55. J.Torrellas. *Incremental Logic Simulation Using Waveforms*, Masters Thesis, Dept. of Electrical and Computer Engineering, University of Wisconsin - Madison, December 1987.

56. J.Beetem and J.Torrellas. *Incremental Logic Simulation Using Waveforms*, technical report ECE-87-5, Univ. of Wisconsin - Madison, April 1987.

Patents

1. "Exploiting Spatial Locality to Reduce Refresh Energy in On-Chip eDRAM Modules", by Aditya B. Agrawal, Amin Ansari, and Josep Torrellas, 2013.

2. ”Exposing Control of Power and Clock Gating for Software”, by Nicholas P. Carter, Joshua B. Fryman, Robert C. Knauerhase, Aditya B. Agrawal, and Josep Torrellas, 2012.

3. ”Architecture Support System and Method for Memory Monitoring”, by Yuanyuan Zhou, Josep Torrellas, and Pin Zhou, US patent number 7,711,988, May 2010.

Editorship of Journals

2013 - 2014 Board of Distinguished Reviewers for the ACM TACO journal.
Mar 03 - Jan 06 Associate Editor, ACM Transactions on Architecture and Code Optimization (TACO).
Dec 01 - Jan 06 Member of the Editorial Board, IEEE Computer Architecture Letters (CAL).

Recent Research Funding

Aug 15 $500 K, NSF CCF, lead PI: J. Torrellas, num PIs: 1.
Title: Architectures for Scripting Languages.
Sep 12 $2.8M ($768K first phase), DARPA PERFECT, lead PI: J. Torrellas, num PIs: 3.
Title: Parameter Variation at NT Voltage: The Power Efficiency versus Resilience Tradeoff.
Sep 12 $8.4M DOE X-Stack + $3.6M cost share, lead PI: S. Borkar, num PIs: 8.
Title: Traleika Glacier X-Stack.
Sep 12 $100K, Mr. Bruce Ge Fund, lead PI: J. Torrellas, num PIs: 1.
Title: Improving Computer Systems.
Sep 11 $2M Intel, plus $1.6M from the University of Illinois, lead PI: J. Torrellas, num PIs: 6.
Title: Illinois-Intel Parallelism Center (I2PC).
Jul 11 $430 K, NSF CSR, lead PI: J. Torrellas, num PIs: 1.
Title: Framework for Concurrency Debugging.
Sep 10 $2.4 M, NSF CCF, lead PI: J. Torrellas, num PIs: 4.
Title: Programmable Many-Core for Extreme Scale Computing.
Jul 10 $25.8M DARPA UHPC, plus $23.2M from Intel, lead PI: S. Borkar, num PIs: 14.
Title: Runnemede: An Architecture for Ubiquitous High Performance Computing.
Aug 10 $1.9 M, DOE ASCR, lead PI: J. Torrellas, num PIs: 4.
Title: Thrifty: An Exascale Architecture for Energy Proportional Computing.
May 10 $70 K, NSF CSR, lead PI: S. King, num PIs: 2.
Title: Supplemental on Deterministic Multiprocessor Replay.
Aug 09 $23 K, DARPA TCTO, lead PI: J. Torrellas, num PIs: 1.
Title: Study on Extreme Scale Multiprocessors.
Jun 09 $168 K, NSF CPA, lead PI: J. Torrellas, num PIs: 3.
Title: Supplemental on Addressing the Parameter Variation Challenge.
Feb 09 $90 K cash + $30 K equipment, Sun Microsystems, lead PI: J. Torrellas, num PIs: 9.
Title: UIUC OpenSPARC Center of Excellence.
Sep 08 $350 K, NSF CSR, lead PI: S. King, num PIs: 2.
Title: Recording and Deterministically Replaying Shared-memory Multiprocessors.
Mar 08 $120 K cash + $50 K equipment, Sun Microsystems, lead PI: J. Torrellas, num PIs: 9.
Title: UIUC OpenSPARC Center of Excellence.
Feb 08 $6M Intel and Microsoft, plus $4.8M from the University of Illinois, lead PI: M. Snir and W. Hwu, num PIs: 15.
Title: Universal Parallel Computing Research Center (UPCRC).
Sep 07 $890 K, NSF CSR, lead PI: J. Torrellas, num PIs: 5.
Title: Novel Programming Models and Architectures to Simplify Parallel Programming.
Jul 07 $1,200 K, NSF CPA, lead PI: J. Torrellas, num PIs: 3.
Title: Addressing the Parameter-Variation Challenge through Architecture, CAD, and Compilers.
Apr 07 $360 K, Semiconductor Research Corporation, lead PI: J. Torrellas, num PIs: 2.
Title: Timing Faults Due to Parameter Variation.
Nov 04 $40 K cash + $25 K equipment, Intel, lead PI: J. Torrellas, num PIs: 1.
Title: Speculative Multithreading.
Nov 04 $500 K, DOE Extreme Scale Computation, lead PI: J. Nieplocha, num PIs: 6.
Title: Scalable Fault Tolerant Runtime and OS.

Sep 03	$1,000 K, NSF Medium ITR, lead PI: J. Torrellas, num PIs: 4. Title: Automatic Detection and Correction of Bugs.
Jul 03	$3,000 K, DARPA-IPTO/IBM/UIUC, lead PI: J. Torrellas, num PIs: 4. Title: IBM PERCS High-Productivity Computer System.
Apr 03	$14 K, UIUC-CNRS, lead PI: D. Padua, num PIs: 6. Title: Program Optimization.
Jul 02	$100 K, DARPA-IPTO/IBM, lead PI: J. Torrellas, num PIs: 3. Title: IBM PERCS High-Productivity Computer System.
Sep 02	$500 K, DOD, lead PI: M. Snir, num PIs: 2. Title: Superconducting Switch for Teraflop Architecture.
Sep 01	$1,375 K, NSF Medium ITR, lead PI: J. Torrellas, num PIs: 2. Title: Novel Scalable Simulation.
Aug 01	$750 K, NSF-NGS, lead PI: D. Padua, num PIs: 3. Title: Open MP for Networked Computing.
Aug 01	$300 K, NSF-NGS, lead PI: L. Rauchwerger, num PIs: 3. Title: Application Centric Computing.
Jun 01	$2,700 K, DARPA-IPTO, lead PI: J. Torrellas, num PIs: 6. Title: Morphable Multithreaded Memory Tiles (M3T).
Sep 00	$1,900 K, NSF-EIA, lead PI: J. Torrellas, num PIs: 3. Title: FlexRAM: Intelligent Memory Architecture.
Sep 00	$500 K, NSF-ITR, lead PI: J. Torrellas, num PIs: 4. Title: Solving the Protein Folding Problem.
Dec 00	$750 K, IBM, lead PI: D. Reed, num PIs: 4. Donation of a 16-node SP2 machine.
Aug 99	$10 K, NSF-CCR, lead PI: J. Torrellas, num PIs: 1. HPCA travel grant.
Sep 99	$300 K, NSF-NGS, lead PI: L. Rauchwerger, num PIs: 3. Title: Application Centric Computing.
Jun 99	$325 K, NSF-CCR, lead PI: J. Torrellas, num PIs: 1. Title: New Architectures to Run Commercial Workloads.
Sep 99	$15 K, IBM, lead PI: J. Torrellas, num PIs: 1. Joint study.
Feb 98	$75 K in cash and $60 K in equip, Intel, lead PI: J. Torrellas, num PIs: 1. Title: Evaluating Database Workloads on Multiprocessors.
Aug 97	$25 K, Commission Scientific Exchange USA-Spain, lead PI: J. Larriba, num PIs: 3. Title: Multiprocessor Computer Architectures and Databases.
Jun 97	$110 K, IBM, lead PI: J. Torrellas, num PIs: 1. IBM Partnership.
Jun 97	$455 K, NSF-MIPS, lead PI: J. Torrellas, num PIs: 2. Title: Illinois Aggressive COMA Multiprocessor.
Jun 96	$100 K, NSF-ASC, lead PI: J. Torrellas, num PIs: 2. Title: Illinois Aggressive COMA Multiprocessor.
Sep 95	$1,213K, DARPA-ITO, lead PI: D. Padua, num PIs: 3. Title: Polaris: A Parallelizing Compiler.

Invited Lectures

- "Improving JavaScript Performance".
  – At Intel Laboratories, Santa Clara, CA, April 2014.

- "Toward Programmable High-Performance Multicores".
  – At University of Washington, Seattle, WA, January 2015.
  – At Stanford University, Stanford, CA, May 2014.
  – At Qualcomm Research, San Jose, CA, December 2013.
  – At University of Cyprus, Nicosia, Cyprus, July 2013.
  – At Technion, Haifa, Israel, June 2013.
  – At Intel Haifa, Israel, June 2013.

– At Princeton University, April 2013.
– At Harvard University, April 2013.
– At Massachussets Institute of Technology, April 2013.
– At University of California Berkeley, April 2013.
– At Intel Laboratories, Santa Clara, CA, April 2013.
– At Carnegie-Mellon University, April 2013.

- "Boosting the Energy Efficiency of Low-Voltage Multicores".
  – At Qualcomm, San Diego, CA, August 2014.
  – At Qualcomm, Raleigh, NC, February 2014.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, January 2014.
  – At AMD, Austin, TX, December 2013.
  – At Intel, Hillsboro, OR, December 2013.

- "Tackling Parameter Variation from an Architectural Perspective".
  – Keynote, at International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Amsterdam, October 2014.

- "Extreme Scale Computer Architecture: Energy Efficiency from the Ground Up".
  – Keynote, at Workshop on Architectures and Systems for Big Data (ASBD), June 2014.
  – At Office of Technology Management, University of Illinois, October 2013.
  – Keynote, IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP), George Washington University Virginia Science and Technology Campus, VA, June 2013.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, February 2013.
  – Invited Speaker, Workshop on Highly-Reliable Power-Efficient Embedded Designs (HARSH), Shenzhen, China, February 2013.
  – At Shanghai Jiao Tong University, Shanghai, February 2013.
  – At National University of Defense Technology (NUDT), Changsha, China, February 2013.
  – At Institute for Computing Technology, Chinese Academy of Sciences, Beijing, December 2012.
  – At Beihang University, Beijing, December 2012.
  – At Tsinghua University, Beijing, December 2012.
  – At Pekin University, Beijing, December 2012.
  – Keynote, Workshop on Near-Threshold Computing (NTC), Vancouver, Canada, December 2012.
  – Jon Postel Distinguished Lecture, Computer Science Department, UCLA, November 2012.

- "Vulcan: Hardware Support for Detecting Sequential Consistency Violations in Programs Dynamically".
  – At I2PC Distinguished Speaker Series, University of Illinois, September 2012.

- "Low Power Architectural Trends".
  – At Nortwestern University, October 2011.

- "Novel Techniques to Debug Multithreaded Programs".
  – At Microsoft Research Asia, Beijing, December 2012.
  – At Intel Programming Systems Laboratory, Santa Clara, CA, October 2010.

- "The Bulk Multicore Architecture for Programmability".
  – At Seoul National University, Seoul, Korea, September 2011.
  – At Samsung, Seoul, Korea, September 2011.
  – At KAIST, Daejeon, Korea, September 2011.
  – At Samsung System LSI division, Seoul, Korea, September 2011.
  – At Pohang University of Science and Technology, Pohang, Korea, September 2011.
  – At University of Florida, Gainesville, FL, February 2011.
  – At University of Michigan, Ann Arbor, MI, April 2010.
  – Keynote, at 4th Workshop on Chip Multiprocessor Memory Systems and Interconnects, Bangalore, India, January 2010.
  – At Intel, Bangalore, India, January 2010.
  – At DARPA-IPTO, Washington, DC, October 2008.

– At Stanford University, Stanford, CA, October 2008.
– At Intel Laboratories, Hillsboro, OR, October 2008.
– At Sun Microsystems, Santa Clara, CA, October 2008.
– At UIUC-UPCRC Research Seminar, Urbana, IL, October 2008.
– At Microsoft Research, Redmond, WA, September 2008.
– At Intel Laboratories, Santa Clara, CA, August 2008.
– At Institute for Computing Technology, Chinese Academy of Sciences, Beijing, June 2008.
– At Tsinghua University, Beijing, June 2008.
– At Beijing University of Aeronautics and Astronautics, Beijing, June 2008.
– At Microsoft Research, Beijing, June 2008.
– At IBM Research, Beijing, June 2008.
– At Intel Laboratories, Barcelona, June 2008.
– At Carnegie Mellon University, June 2008.
– At University of California Berkeley, May 2008.
– At Massachussets Institute of Technology, May 2008.
– At Harvard University, May 2008.
– At IBM T.J. Watson Research Center, Yorktown, NY, May 2008.
– At Texas A&M University, April 2008.
– At Georgia Institute of Technology, April 2008.
– At University of Texas at Austin, April 2008.
– At University of Tokyo, April 2008.
– At Rice University, April 2008.

- ”Parameter Variation-Tolerant Computer Architectures”.
  – Distinguished Speaker Colloquium, ECE Department, North Carolina State University, Raleigh, NC, March 2012.
  – At IBM Research, Austin, TX, February 2011.
  – At University of Minnesota, Minneapolis, MN, December 2010.
  – At Intel, Marlborough, MA, January 2009.
  – Keynote, at Los Alamos Computer Science Symposium (LACSS), Santa Fe, October 2008.
  – At Department of Computer Science Distinguished Lectures, UIUC, Urbana, IL, October 2008.
  – Keynote, at Workshop on Quality-Aware Design, June 2008.
  – At Intel Microarchitecture Research Laboratory, Hillsboro, OR, March 2008.
  – Invited Talk at IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips X), Yokohama, Japan, April 2007.
  – At Waseda University, Tokyo, April 2007.
  – Invited Talk at Third IBM TJ Watson Conference on Interaction between Architecture, Circuits and Compilers (PAC2), October 2006.
  – At Department of Electrical and Computer Engineering, University of Toronto, December 2005.
  – At VLSI Circuits Seminar, Department of Electrical and Computer Engineering, UIUC, October 2005.

- ”An Agenda for Parallel Computer Architecture and Parallel Computing”.
  – At Texas A&M University, April 2009.

- ”Practical Deterministic Multiprocessor Replay”.
  – At Intel Laboratories, Santa Clara, CA, December 2009.
  – At Microsoft, Redmond, WA, April 2009.
  – At Intel, Hillsboro, OR, April 2009.

- ”Designing Multicores for Single-Thread Performance”.
  – At IBM T.J. Watson Research Center, Yorktown, NY, February 2009.
  – At Sun Microsystems, Santa Clara, CA, December 2008.

- ”Speculative Multithreading Architectures”.
  – At Intel Microarchitecture Research Laboratory, Hillsboro, OR, August 2006.

- "A Near-Memory Processor for Vector, Streaming and Bit Manipulation Workloads".
  – At IBM PERCS Virtual Seminar, January 2005.

- "Hardware-Supported Data Race Detection".
  – At Intel, Champaign, IL, April 2005.
  – At Intel, Champaign, IL, November 2004.

- "Using Thread Level Speculation for Performance and to Enhance Software Debugging and Programmability".
  – At Cornell University, Ithaca, NY, November 2004.
  – At SUN Microsystems, Sunnyvale, CA, August 2004.
  – At Intel, Champaign IL, January 2004.
  – At Universidad Complutense de Madrid, Spain, June 2003.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, April 2003.
  – At Intel Microprocessor Research Laboratory, Santa Clara CA, March 2003.

- "Challenging Issues in Speculative Multithreading".
  – At Carnegie-Mellon University, Pittsburgh PA, December 2002.
  – At University of Rochester, Rochester NY, December 2002.
  – At Intel, Marlborough, MA, May 2002.
  – At Compaq Computer, Shrewsbury, MA, May 2002.
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, July 2000.

- "FlexRAM: Toward an Advanced Intelligent Memory System".
  – At Los Alamos National Laboratory, Los Alamos NM, September 2002.
  – At Purdue University, West Lafayette, IN, April 2002.
  – At Intel, Champaign IL, December 2001.
  – Keynote Speech at XII Jornadas Nacionales de Paralelismo, Valencia, Spain, September 2001.
  – At Los Alamos National Laboratory, Los Alamos NM, March 2001.
  – At Massachusetts Institute of Technology (MIT), February 2001.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, October 2000.
  – At Universidad Politecnica de Madrid, Spain, January 2000.
  – At Chalmers University, Gothenburg, Sweden, December 1999.
  – At Intel Corporation, Hillsboro, OR, November 1999.
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, August 1999.
  – At Univeriste de Versailles, France, July 1999.
  – At DARPA ITO Data Intensive Systems PI Meeting, Del Mar, CA, February 1998.

- "New Research Topics in Computer Architecture".
  – At Universidad de Zaragoza, Zaragoza, Spain, June 2002.

- "A Framework for Dynamic Energy Efficiency and Temperature Management".
  – At Universitat Politecnica de Catalunya, Barcelona, December 2000.

- "Upcoming Architectural Advances in DSM Machines and Their Impact on Programmability".
  – At Institute for Scientific Computing, Aachen, Germany, August 1999.

- "Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors".
  – At Dagstuhl Seminar, Dagstuhl, Germany, August 2002.
  – At National Center for Supercomputing Applications (NCSA), Urbana, IL May 1999.

- "New Trends in Computer Architecture and the i-ACOMA Scalable Multiprocessor Project".
  – At NEC Corporation, Fuchu City, Japan, September 1999.
  – At Waseda University, Tokyo, Japan, September 1999.
  – At University of Houston, Houston, TX, January 1999.
  – At Universidade de A Corunha, A Coruhna, Spain, December 1998.
  – At Universidade de Santiago, Santiago, Spain, December 1998.
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, December 1998.

– At New York University, NY, October 1998.
– At DARPA, Washington, DC, September 1998.
– At NSF, Washington, DC, September 1998.
– At the National Center for Supercomputing Applications, Urbana, IL, May 1998.
– At Intel Corporation, Hillsboro, OR, April 1998.
– At VLSI Circuits Seminar, University of Illinois at Urbana Champaign, April 1998.

- "Efficient Execution of Database Workloads under Deep Memory Hierarchies".
  – At Pennsylvania State University, State College, PA, November 1998.
  – At Oracle Corporation, Redwood Shores, CA, February 1998.
  – At Hewlett Packard Laboratories, Palo Alto, CA, February 1998.

- "New Results in the Illinois Aggressive COMA Multiprocessor Project".
  – At Los Alamos National Laboratory, Los Alamos NM, May 1998.
  – At Hewlett Packard Laboratories, Palo Alto, CA, February 1998.
  – At Texas A&M University, College Station, TX, January 1998.
  – At Convex Computer, Dallas, TX, January 1998.
  – At Northwestern University, Evanston, IL, December 1997.
  – At University of Washington, Seattle, WA, October 1997.
  – At Carnegie-Mellon University, Pittsburgh, PA, October 1997.
  – At Sequent Computers, Hillsboro, OR, April 1997.
  – At Silicon Graphics, Mountain View, CA, January 1997.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, November 1996.

- "Exploiting Billion-Transistor Chips for Multiprocessing".
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, December 1997.
  – At Reflections/Projections ACM Student Chapter Conference, Urbana, IL, October 1997.

- "The Illinois Aggressive COMA Multiprocessor".
  – At Department of Computer Science, Tsinghua University, Beijing, China, January 1997.
  – At University of California-Berkeley, Berkeley, CA, February 1996.
  – At Stanford University, Stanford, CA, February 1996.
  – At Tandem Computers, Cupertino, CA, August 1995.
  – At SUN Microsystems, Mountain View, CA, August 1995.
  – At Universidad Politecnica de Valencia, Valencia, Spain, June 1995.
  – At Universite Paul Sabatier, Toulouse, France, June 1995.
  – At Intel Scalable Systems Division, Intel Corporation, Beaverton, OR, May 1995.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, February 1995.
  – At Digital Equipment Corporation, Hudson, MA, February 1995.
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, December 1994.

- "The Performance of the Cedar Multistage Interconnection Network".
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, December 1993.

- "The Cache Performance of Multiprocessor Operating Systems".
  – At Hewlett-Packard, Cupertino, CA, May 1992.
  – At Silicon Graphics Inc., Mountain View, CA, January 1992.
  – At SUN Microsystems Computer Corp., Palo Alto, CA, October 1991.

Conference Organization. Steering Committee

Jul 05	-	pres.	IEEE/ACM International Symposium on Computer Architecture (ISCA).
Jul 05	-	pres.	IEEE International Symposium on High-Performance Computer Architecture (HPCA).
Apr 06	-	Feb 08	ACM Symposium on Principles and Practice of Parallel Programming (PPoPP).
Sep 05	-	Oct 07	IEEE/ACM International Conference on Parallel Architectures and Compilation Techniques (PACT).
Aug 14	-	pres.	PACT.

Conference Organization. Chair

- Program Chair. The 23rd International Conference on Parallel Architectures and Compilation Techniques (PACT), Edmonton, Canada, August 2014.
- Program Chair. The 39th International Symposium on Computer Architecture (ISCA), Portland, OR, June 2012.
- Vice-General Chair. IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), Yokohama, Japan, 2008-2016.
- General Co-Chair. International Conference on Network and Parallel Computing (NPC), Shanghai, China, October 2008.
- Technical Papers Co-Chair. IEEE/ACM International Conference for High Performance Computing, Networking, Storage, and Analysis (SC07), Reno, NV, November 2007.
- General Chair. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), New York, NY, March 2006.
- Program Chair. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences, January-February 2006.
- General Chair. International Conference on Parallel Architectures and Compilation Techniques (PACT), Saint Louis, MO, September 2005.
- Program Chair. The 11th International Symposium on High-Performance Computer Architecture (HPCA), San Francisco, CA, February 2005.
- Architecture Area Chair. International Conference for High Performance Computing Networks and Storage (SC03), Phoenix, AZ, November 2003.
- Program Vice-Chair for Architecture. The 17th International Parallel and Distributed Processing Symposium (IPDPS), Nice, France, April 2003.
- Vice-Chair of Architecture. The 2001 International Conference on Parallel Processing (ICPP), Valencia, Spain, September 2001.
- General Co-Chair. The 6th International Symposium on High-Performance Computer Architecture (HPCA), Toulouse, France, January 2000.
- Minitrack Organizer. Minitrack on Scalable Shared-Memory Architectures. The 28th Hawaii International Conference on System Sciences (HICSS), Hawaii, January 1995.

Conference Organization. Program Committee

– External Program Committee Member. International Symposium on High Performance Computer Architecture (HPCA), Barcelona, Spain, March 2016.
– External Program Committee Member. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Atlanta, GA, April 2016.
– External Program Committee Member. International Symposium on Microarchitecture (MICRO), Waikiki, HI, December 2015.
– External Program Committee Member. International Symposium on Computer Architecture (ISCA), Portland, OR, June 2015.
– Program Committee Member. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences, May-June 2015.
– External Program Committee Member. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Istanbul, Turkey, March 2015.
– Program Committee Member. The 21st International Symposium on High-Performance Computer Architecture (HPCA), San Francisco, CA, February 2015.
– External Program Committee Member. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Salt Lake City, UT, March 2014.

– Program Committee Member. The 40th International Symposium on Computer Architecture (ISCA), Tel Aviv, Israel, June 2013.
– Program Committee Member. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences, May-June 2013.
– External Program Committee Member. International Symposium on Microarchitecture (MICRO), Vancouver, Canada, December 2012.
– Program Committee Member. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences, May-June 2012.
– External Program Committee Member. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), London, UK, March 2012.
– Program Committee Member. The 18th International Symposium on High-Performance Computer Architecture (HPCA), New Orleans, LA, February 2012.
– Program Committee Member. International Conference on Parallel Architectures and Compilation Techniques (PACT), Galveston Island, TX, October 2011.
– Program Committee Member. The 38th International Symposium on Computer Architecture (ISCA), San Jose, CA, June 2011.
– External Program Committee Member. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Newport Beach, CA, March 2011.
– Program Committee Member. The 17th International Symposium on High-Performance Computer Architecture (HPCA), San Antonio, TX, February 2011.
– Technical Papers Committee Member. International Conference for High Performance Computing Networks and Storage (SC), November 2010.
– Program Committee Member. The 37th International Symposium on Computer Architecture (ISCA), Saint Malo, France, June 2010.
– External Program Committee Member. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Pittsburgh, PA, March 2010.
– Program Committee Member. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences, January-February 2010.
– Program Committee Member. The 16th International Symposium on High-Performance Computer Architecture (HPCA), Bangalore, India, January 2010.
– Program Committee Member. The 36th International Symposium on Computer Architecture (ISCA), Austin, TX, June 2009.
– Program Committee Member. The 15th International Symposium on High-Performance Computer Architecture (HPCA), Raleigh, NC, February 2009.
– Program Committee Member. Architecture Track. IEEE/ACM International Conference for High Performance Computing, Networking, Storage, and Analysis (SC), Austin, TX, November 2008.
– Program Committee Member. The 35th International Symposium on Computer Architecture (ISCA), Beijing, China, June 2008.
– Program Committee Member. The 14th International Symposium on High-Performance Computer Architecture (HPCA), Salt Lake City, UT, February 2008.
– Program Committee Member. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences, January-February 2008.
– Program Committee Member. International Conference on High Performance Embedded Architectures and Compilers (HIPEAC), Goteborg, Sweden, January 2008.
– Program Committee Member. The 34th International Symposium on Computer Architecture (ISCA), San Diego, CA, June 2007.
– Program Committee Member. The 33rd International Symposium on Computer Architecture (ISCA), Boston, MA, June 2006.
– Program Committee Member. The 12th International Symposium on High-Performance Computer Architecture (HPCA), Austin, TX, February 2006.
– Technical Papers Committee Member. International Conference for High Performance Computing Networks and Storage (SC05), Seattle, WA, November 2005.
– Program Committee Member. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), Chicago, IL, June 2005.

– Program Committee Member. Industrial Perspectives on Challenges for Next-Generation Computer Systems, The 11th International Symposium on High-Performance Computer Architecture, (HPCA), San Francisco, CA, February 2005.
– Program Committee Member. The 37th Annual International Symposium on Microarchitecture (MICRO), Portland, OR, December 2004.
– Publications Chair. International Conference on Parallel Architectures and Compilation Techniques (PACT), Antibes, France, September 2004.
– Program Committee Member. The 31st Annual International Symposium on Computer Architecture (ISCA), Munich, Germany, June 2004.
– Program Committee Member. The 10th International Symposium on High-Performance Computer Architecture (HPCA), Madrid, February 2004.
– Program Committee Member. The 36th Annual International Symposium on Microarchitecture (MICRO), San Diego, December 2003.
– Program Committee Member. The 17th ACM International Conference on Supercomputing (ICS), San Francisco, June 2003.
– Program Committee Member. The 9th International Symposium on High-Performance Computer Architecture (HPCA), Anaheim, CA, February 2003.
– Technical Papers Committee Member. International Conference for High Performance Computing Networks and Storage (SC02), Baltimore, MD, November 2002.
– Program Committee Member. The 8th International Symposium on High-Performance Computer Architecture (HPCA), Boston, February 2002.
– Program Committee Member. The 16th International Parallel and Distributed Processing Symposium (IPDPS), Fort Lauderdale, FL, April 2002.
– Finance Chair. International Conference on Parallel Architectures and Compilation Techniques (PACT), Barcelona, September 2001.
– Program Committee Member. The 28th Annual International Symposium on Computer Architecture (ISCA), Goteborg, Sweden, June 2001.
– Tutorials Chair. The 28th Annual International Symposium on Computer Architecture (ISCA), Goteborg, Sweden, June 2001.
– Program Committee Member. 15th International Parallel and Distributed Processing Symposium (IPDPS), San Francisco, April 2001.
– Program Committee Member. The 7th International Symposium on High-Performance Computer Architecture (HPCA), Monterrey, Mexico, January 2001.
– Publicity Chair. International Conference on High Performance Computing (HIPC), India, December 2000.
– Program Committee Member. International Conference on Parallel Architectures and Compilation Techniques (PACT), Philadelphia, October 2000.
– Program Committee Member. The 2000 International Conference on Parallel Processing (ICPP), Toronto, Canada, August 2000.
– Program Committee Member. The International Conference on High Performance Computing (HIPC99), India, December 1999.
– Program Committee Member. The 13th ACM International Conference on Supercomputing (ICS), Rhodes, Greece, June 1999.
– Program Committee Member. The 1999 International Conference on Parallel Processing (ICPP), Aizu-Wakamatsu, Fukushima, Japan, September 1999.
– Program Committee Member. The 7th IEEE Symposium on the Frontiers of Massively Parallel Processing (Frontiers'99), Annapolis, Maryland, February 1999.
– Program Committee Member. The 5th International Symposium on High-Performance Computer Architecture (HPCA), Orlando, FL, January 1999.
– Program Committee Member. The 1998 International Conference on Parallel Processing (ICPP), Minneapolis, MN, August 1998.
– Workshops Chair. The 25st Annual International Symposium on Computer Architecture (ISCA), Barcelona, Spain, June 1998.
– Program Committee Member. The 1998 ACM Sigmetrics Conference, Madison WI, June 1998.
– Program Committee Member. The 1998 International Parallel Processing Symposium (IPPS), Orlando FL,

March 1998.
– Workshops and Tutorials Chair. 4th International Symposium on High-Performance Computer Architecture (HPCA), Las Vegas, February 1998.
– Program Committee Member. The 4th International Symposium on High-Performance Computer Architecture (HPCA), Las Vegas, February 1998.
– Program Committee Member. The 1997 International Conference on Parallel Processing (ICPP), Chicago, IL, August 1997.
– Program Committee Member. The 11th ACM International Conference on Supercomputing (ICS), Vienna, Austria, July 1997.
– Program Committee Member. The 6th IEEE Symposium on the Frontiers of Massively Parallel Processing (Frontiers'96), Annapolis, Maryland, October 1996.
– Program Committee Member. The 10th ACM International Conference on Supercomputing (ICS), Philadelphia, Pennsylvania, May 1996.
– Registration Chair. 2nd International Computer Performance and Dependability Symposium (ICPDS), Urbana IL, September 1996.
– Program Committee Member. The 15th International Conference of the Chilean Computer Science Society (ICCCSS), Arica, Chile, November 1995.
– Program Committee Member. The 15th International Conference on Distributed Computing Systems (ICDCS), Vancouver, Canada, May 1995.
– Program Committee Member. 1st International Computer Performance and Dependability Symposium (ICPDS), Erlangen, Germany, April 1995.
– Program Committee Member. The 14th International Conference on Distributed Computing Systems (ICDCS), Poznan, Poland, June 1994.
– Registration Chair. The 21st Annual International Symposium on Computer Architecture (ISCA), Chicago, IL, April 1994.

Workshop Organization. Chair

- Program Co-Chair. Workshop on "Managing Overprovisioned Processors", Salt Lake City, UT, March 2014.
- Program Chair. "2013 Illinois Symposium on Parallelism: Current State of the Field and the Future", Urbana, IL, September 2013.
- Program Co-Chair. Workshop on Advancing Computer Architecture Research (ACAR). "What Now in ILP Research?", Seattle, WA, September 2010.
- Program Co-Chair. Workshop on Advancing Computer Architecture Research (ACAR). "Failure is not an Option: Popular Parallel Programming", San Diego, CA, February 2010.
- Program Co-Chair. Intel/Microsoft/Illinois/Berkeley Universal Parallel Computing Research Center (UPCRC).
  – Workshop on Architecture, Santa Clara, CA, August 2011.
  – Workshop on Power Issues, Urbana, IL, April 2011.
  – Workshop on Architectures for Fine-Grain Synchronization, Redmond, WA, August 2010.
  – Workshop on Compilation for Block-Based Architectures, Urbana, IL, March 2010.
  – Workshop on Multicore Architectures for Programmability, Hillsboro, OR, August 2009.
  – Workshop on Multicore Computer Architecture for 2015, Urbana, IL, February 2009.
  – Workshop on Computer Architecture, Santa Clara, CA, August 2008
- Program Co-Chair. "Indo-US Workshop on Parallelism and the Future of High-Performance Computing", Bangalore, India, January 2010.
- Program Co-Chair. "First Workshop on Architectural and System Support for Improving Software Dependability" (ASID). In conjunction with ASPLOS-XII, San Jose, CA, October 2006.
- Program Co-Chair. "Second Workshop on Memory Performance Issues" (WMPI 2002). In conjunction with ISCA-29, Achorage, Alaska, May 2002.

- Program Co-Chair. "First Workshop on Memory Performance Issues" (WMPI 2001). In conjunction with ISCA-28, Goteborg, Sweden, June 2001.
- Program Co-Chair. "Ninth Workshop on Scalable Shared Memory Multiprocessors". In conjunction with ISCA-27, Vancouver, June 2000.
- Program Co-Chair. "Eighth Workshop on Scalable Shared Memory Multiprocessors". In conjunction with ISCA-26, Atlanta, GA, May 1999.
- Program Co-Chair. "Seventh Workshop on Scalable Shared Memory Multiprocessors". In conjunction with ISCA-25, Barcelona, June 1998.
- Program Co-Chair. "Fourth Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-7, Monterrey, Mexico January 2001.
- Program Co-Chair. "Third Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-6, Toulouse, France January 2000.
- Program Co-Chair. "Second Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-5, Orlando, January 1999.
- Program Co-Chair. "First Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-4, Las Vegas, February 1998.
- Program Chair. Birds-of-a-Feather Session on "Future Machine Architecture and Organization", at the National Computational Science Alliance (NCSA) Alliance'98, Urbana, IL, April 1998.

Workshop Organization. Program Committee

– Program Committee Member. Workshop on Near-Threshold Computing (WNTC), Portand, OR, June 2015.
– Program Committee Member. Workshop on Determinism and Correctness in Parallel Programming (WODET), Houston, TX, March 2013.
– Program Committee Member. Workshop on Near-Threshold Computing (WNTC), Vancouver, Canada, December 2012.
– Program Committee Member. Workshop on Hardware Support for Parallel Program Correctness, Porto Alegre, Brazil, December 2011.
– Program Committee Member. The 3rd Workshop on System Effects of Logic Soft Errors (SELSE-III), Austin, TX, April 2007.
– Program Committee Member. The 1st Workshop on Multithreaded Architectures and Applications (MTAAP), Long Beach, CA, March 2007.
– Program Committee Member. The 2nd Workshop on System Effects of Logic Soft Errors (SELSE-II), Urbana, IL, April 2006.
– Program Committee Member. The 3rd Workshop on Power-Aware Computer Systems (PACS), San Diego, December 2003.
– Program Committee Member. 6th Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC), Istambul, Turkey, November 2002.
– Program Committee Member. 5th Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC), Austin, December 2001.
– Program Committee Member. 4th Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC), Monterey, December 2000.
– Program Committee Member. The 2nd Workshop on Intelligent Memory Systems, Boston, November 2000.
– Program Committee Member. 3rd Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC), Toulouse, France, January 2000.
– Program Committee Member. 2nd Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC), Orlando, FL, January 1999.

Tutorials and Short Courses

- Course on "Modern Shared-Memory Parallel Computer Architecture", at Beihang University, Beijing, China, December 2012. 12 hours.

- ”High Performance Computing Architectures – Trends and Directions”, course at UIUC Course on High Performance Computing, Singapore, June 2010.
- ”Parallel@Illinois Symposium at Singapore”, Singapore, June 2010.
- ”Multiprocessor Architectures for Speculative Multithreading”, course at Fourth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), L’Aquila, Italy, July 2008.
- ”Boosting Machine Performance with Thread-Level Speculation”, course at Cursos de Verano, Universidad Complutense de Madrid, El Escorial, Spain, July 2004.
- ”New Technologies in Computer Architecture”, course at Universidad de Zaragoza, Spain, June 2002.
- ”Performance Modeling Using Hardware Counters”, tutorial at at International Symposium on High-Performance Computer Architecture (HPCA), Toulouse, France, January 2000.
- ”Scalable Shared-Memory Multiprocessors”, course at Universitat Politecnica de Catalunya, Barcelona, Spain, July 1998.
- ”Scalable Shared-Memory Multiprocessors: Architecture and Implementation Issues”, tutorial at VII Jornadas de Paralelismo, Santiago, Spain, September 1996.

Panels Organized

- ”Broadening Computer Architecture Research: Embracing New Areas to Keep the Field Vibrant”, International Symposium on Computer Architecture, San Jose, CA, June 2011.
- ”Extreme Scale Computing: Challenges and Opportunities”, International Symposium on High-Performance Computer Architecture and International Conference on Principles and Practice of Parallel Programming, Bangalore, India, January 2010.
- ”High-Performance Architecture Research”, Indo-US Workshop on Parallelism and the Future of High-Performance Computing, Bangalore, India, January 2010.
- ”Speculative Multithreading Architectures”, Minipanel at International Symposium on Computer Architecture, Austin, TX, June 2009.
- ”How to Build a Useful Thousand-Core Manycore System?”, IEEE International Parallel and Distributed Processing Symposium (IPDPS), Rome, Italy, May 2009.
- ”Multi-Core and Many-Core: the 5 to 10 Year View”, IEEE Symposium on Low-Power and High-Speed Chips, Yokohama, Japan, April 2009.
- ”Wish List: Architectural Support and Tool Infrastructure for Improving Software Dependability”, Workshop on Architectural and System Support for Improving Software Dependability (ASID), in conjunction with ASPLOS-XII, San Jose, CA, October 2006.
- ”An Agenda for Computer Architecture Research on Hardware Complexity”, Workshop on Complexity-Effective Design (WCED), in conjunction with ISCA-33, Boston, MA, June 2006.
- ”Soft Error Rate (SER) Scaling Trends”, Workshop on System Effects of Logic Soft Errors (SELSE), Urbana-Champaign, IL, April 2006.
- ”New Technologies in Computer Architecture”, Dagstuhl Seminar on Performance Analysis and Distributed Computing (PADC), Dagstuhl, Germany, August 2002.
- ”What’s the Most Critical Challenge is Supporting Multimedia Applications”, The 2001 International Conference on Parallel Processing (ICPP), Valencia, Spain, September 2001.

- "Designing Scalable Shared-Memory Multiprocessors Using Commodity Microprocessors and OS: NUMA vs COMA Implementation", Fifth Workshop on Scalable Shared-Memory Multiprocessors, Santa Margherita, Italy, June 1995.

Participation in Panels

– "Architecture and System for Big Data Processing", Workshop on Architectures and Systems for Big Data (ASBD), Minneapolis, MN, June 2014.
– "Future Applications and Challenges for NTC", Workshop on Near-threshold Computing, Minneapolis, MN, June 2014.
– "The Future of Parallelism", 2013 Illinois Symposium on Parallelism: Current State of the Field and the Future, Urbana, IL, September 2013.
– "Research Directions for 21st Century Computer Systems", International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Houston, TX, March 2013.
– "Future of Computing Systems", IBM T.J. Watson Research Center, Yorktown Heights, NY, February 2013.
– "Is Reliability the Main Roadblock to Ultra-Low Voltage Operation?", Workshop on Near-threshold Computing (WNTC), Vancouver, Canada, December 2012.
– "Many Core – Does It Work?", 8th Workshop on Duplicating, Deconstructing, and Debunking (WDDD), Austin, TX, June 2009.
– "How to Place Students in Top-5 Departments", Department of Computer Science, UIUC, April 2009.
– "Silicon Errors in Modern Integrated Circuits: What are the Main Threats", Third Workshop on System Effects of Logic Soft Errors (SELSE-III), Austin, IL, April 2007.
– "Chip Design in the Nano Era", International Conference on Computer Aided Design (ICCAD), San Jose, CA, November 2005.
– "What Are the Important Research Challenges in Temperature-Aware Computer Systems?", Second Workshop on Temperature-Aware Computer Systems, Madison, WI, June 2005.
– "Current and Future Processors", Cursos de Verano, Universidad Complutense de Madrid, El Escorial, Spain, July 2004.
– "Research Challenges for the Architecture Community in Temperature-Aware Design", First Workshop on Temperature-Aware Computer Systems, Munich, Germany, June 2004.
– "New Architectural Technologies", DOE Salishan High Speed Computing Conference, Salishan Lodge, Gleneden Beach, OR, April 2004.
– "What does the Future Hold for Parallel Languages?", The 16th International Workshop on Languages and Compilers for Parallel Computing, College Station, TX, October 2003.
– "Future Architectures and Programming Models for High Performance Computing", International Symposium on Principles and Practice of Parallel Programming (PPoPP), San Diego, June 2003.
– "Research in Computer Architecture", XII Jornadas Nacionales de Paralelismo, Valencia, Spain, September 2001.
– "Microprocessor Design Beyond the PC Era: Is There Room for Innovation?", 15th International Parallel and Distributed Processing Symposium (IPDPS), San Francisco, April 2001.
– "What Tools Do We Use to Evaluate Future Memory Systems?", Third Workshop on Computer Architecture Evaluation Using Commercial Workloads, Toulouse, France, January 2000.
– "Findings of the Petaflop Workshops", The 7th IEEE Symposium on the Frontiers of Massively Parallel Processing (Frontiers'99), Annapolis, MD, February 1999.
– "Issues in Petaflop Machines", The Third PetaFlop Workshop (TPF-3), Annapolis, MD, February 1999.
– "Cooperation Between Industry, Academia and Government to Make Commercial Applications Widely Available", 2nd Workshop on Computer Architecture Evaluation Using Commercial Workloads, Orlando, FL, January 1999.
– "Microbenchmarks: Risk versus Utility", Workshop on Performance Analysis and its Impact on Design (PAID), Barcelona, June 1998.
– "The First Course: Bottom-Up or Top-Down? Which is More Effective?", Fourth Workshop on Computer Architecture Education, Las Vegas, NV, January 1998.
– "Do Academics Require Access to DBMS Source Code in Order To Do Effective Research in the Area of Computer Architecture for Commercial Workloads?", First Workshop on Computer Architecture Evaluation Using Commercial Workloads, Las Vegas, NV, January 1998.
– "Multiprocessor Applications for IRAM", First Workshop on Mixing Logic and DRAM: Chips that Compute and Remember, Denver, CO, June 1997.

– ”Paths to the Petaflops Architecture”, The 6th Symposium on the Frontiers of Massively Parallel Computation (Frontiers’96), Annapolis, Maryland, October 1996.
– ”Shared-Disk, Shared-Nothing, and Shared-Memory Architectures”, First Intel Server Forum, Hillsboro OR, June 1996.
– ”What are the Minimal Elements of a Computer Engineering or Computer Science Curriculum?”, 2nd Annual Workshop on Computer Architecture Education, San Jose, California, February 1996.
– ”Hot Research Topics in Processor Architecture and in Shared Memory Multiprocessor Architecture”, 1st Workshop on Computer Architecture, Paris, France, June 1995.

Talks at Workshops

– ”What the Parallelism Center Accomplished”, at 2013 Illinois Symposium on Parallelism: Current State of the Field and the Future, Urbana, IL, September 2013.
– ”Parameter Variation at NT Voltage: The Power Efficiency versus Resilience Tradeoff”, at DARPA PERFECT Program Meeting, Arlington, VA, February 2013.
– ”The Illinois Parallelism Center”, at Microsoft Faculty Summit, Seattle, WA, July 2012.
– ”Toward Programmable Extreme Scale Computing”, NSF/CISE Workshop on Cross-Layer Power Optimization and Management (CPOM), Los Angeles, CA, February 2012.
– ”Thrifty: An Exascale Architecture for Energy-Proportional Computing”, at Exascale Research Meeting, DOE Office of Advanced Scientific Computing Research, San Diego, CA, March 2011.
– ”Accelerating Single-Thread Execution with Low Design Complexity: The BubbleWrap Approach”, at Workshop on Advancing Computer Architecture Research (ACAR), What Now in ILP Research?, Seattle, WA, Sept. 2010.
– ”Update on the Bulk Multicore Architecture”, at Universal Parallel Computing Research Center (UPCRC) and Illinois Intel Parallelism Center (I2PC) Summits and Workshops: Santa Clara, CA (August 2008); Urbana, IL (February 2009); Hillsboro, OR (August 2009); Urbana, IL (March 2010); Seattle, WA (August 2010); Urbana, IL (April 2011); Santa Clara, CA (August 2011); Hillsboro, OR (December 2011); Seattle, WA (July 2012); Santa Clara, CA (August 2012); Urbana, IL (September 2013).
– ”The Architecture Needs to be Designed for Programmability”, at Workshop on Advancing Computer Architecture Research (ACAR), Failure is not an Option: Popular Parallel Programming, San Diego, CA, February 2010.
– ”High-Speed, Transparent, Scalable Checkpointing”, at Intel Workshop on New Memory Technologies, Hillboro, OR, January 2010.
– ”Simple Architectural Support to Check for Determinism”, at Workshop on Determinism, Seattle, WA, December 2009.
– ”The Bulk Compiler”, Intel/Microsoft/Illinois/Berkeley UPCRC Workshop on Multicore Architectures for Programmability, Hillsboro, OR, August 2009.
– ”Extreme Scale Architectures for Programmability”, at DARPA-IPTO Workshop on Ubiquitous High Performance Computing, Stanford, CA, August 2009.
– ”High-Performance Parallel Computer Architectures”, at Workshop on Careers in High Performance Systems Mentoring, Urbana, IL, July 2009.
– ”Multiprocessor Architectures for Programmability”, at DARPA-IPTO Workshop on Exascale Ubiquitous High Performance Computing, University of Notre Dame, IN, April 2009.
– ”The Bulk Multicore Architecture for Programmability”, at Intel/Microsoft/Illinois/Berkeley UPCRC Workshop on Multicore Computer Architecture for 2015, Urbana, IL, February 2009.
– ”The Bulk Multicore Architecture for Programmability”, at Intel/Microsoft/Illinois/Berkeley UPCRC Workshop on Computer Architecture, Santa Clara, CA, August 2008.
– ”How Do We Use 50-Billion Transistors on a Chip?”, at Workshop on The 50 Billion Transistor Challenge, IBM T.J. Watson Research Center, Yorktown Heights, NY, July 2008.
– ”An Updated Evaluation of ReCycle”, at Workshop on Duplicating, Deconstructing, and Debunking, Beijing, China, June 2008.
– ”Speculative Multithreaded Architectures”, at Workshop on Architectures and Compilers for Multithreading, Indian Institute of Technology, Kanpur, India, December 2007.
– ”Terascale-Level Multicore Processor Architectures: Promises and Roadblocks”, at Workshop on Terachip Codesign, Defense Science Research Council (DSRC), Arlington, VA, October 2007.
– ”Colorama: Supporting the Data-Centric Synchronization Model”, at Workshop on Directions in Multi-Core Processor Research, Microsoft Research, Redmont, WA, January 2007.
– ”Metrics for Processor Complexity”, at Workshop on Complexity-Effective Design (WCED), in conjunction with ISCA, June 2005.

– ”Modern Rollback Techniques”, at DARPA-Sponsored Information Science and Technology (ISAT) Study on Law of Large Numbers System Design, Menlo Park, CA, February 2005.
– ”New Architectural Technologies for Shared-Memory Systems”, at DOE Salishan High Speed Computing Conference, Salishan Lodge, Gleneden Beach, OR, April 2004.
– ”The FlexRAM Intelligent Memory System”, at the Workshop on the Implementation of Multi-PIM Systems (WIMPS), Bodega Bay, CA, February 2002.
– ”Hardware for Speculative Parallelization in High-End Multiprocessor”, at The Third PetaFlop Workshop (TPF-3), Annapolis, MD, February 1999.
– ”New Multithreading Architectures”, at Internal IBM Workshop on Next Generation Processor Architectures, IBM Rochester, Rochester, MN, September 1998.
– ”Hardware for Speculative Parallelization in Large- and Small-Scale Multiprocessors”, at Seventh Workshop on Scalable Shared Memory Multiprocessors, Barcelona, June 1998.
– ”Compiler Support for Data Forwarding in Scalable Shared-Memory Multiprocessors”, at Seventh Workshop on Scalable Shared Memory Multiprocessors, Barcelona, June 1998.
– ”Computer Architecture Education at the University of Illinois”, at 5th Annual Workshop on Computer Architecture Education, Barcelona, Spain, June 1998.
– ”COTS-Based Route to Petaflops Systems”, at Petaflops Systems Operations Working Review (POWR), Bodega Bay, CA, June 1998.
– ”FlexRAM: Advanced Intelligent Memory”, at Data Intensive Computing Systems, DARPA PI Meeting, Del Mar, CA, February 1998.
– ”How Processor-Memory Integration Affects the Design of DSMs”, at First Workshop on Mixing Logic and DRAM: Chips that Compute and Remember, Denver, CO, June 1997.
– ”A COTS-Based Petaflops Design”, at 1997 Petaflops Algorithms Workshop (PAL’97), Williamsburg, VA, April 1997.
– ”The Illinois Aggressive Cache Only Memory Architecture Multiprocessor”, at Workshop on the Petaflop Frontier, Annapolis MD, October 1996.
– ”The Illinois Aggressive Cache Only Memory Architecture Multiprocessor”, at First Intel Server Forum, Hillsboro OR, June 1996.
– ”The Illinois Aggressive Cache Only Memory Architecture Multiprocessor”, at Petaflops Architecture Workshop (PAWS’96), Oxnard CA, April 1996.
– ”Computer Architecture Education at the University of Illinois: Current Status and Some Thoughts”, at 2nd Annual Workshop on Computer Architecture Education, San Jose, California, February 1996.
– ”The Illinois Aggressive COMA Multiprocessor”, at 1st Workshop on Computer Architecture, Paris, France, June 1995.
– ”Evaluating the Benefits of Cache-Affinity Scheduling in Shared-Memory Multiprocessors”, at Third Workshop on Scalable Shared-Memory Multiprocessors, San Diego, CA, May 1993.
– ”The Cache Behavior of Shared Data in Cache-Coherent Multiprocessors”, at First Workshop on Scalable Shared Memory Multiprocessors, Seattle, WA, May 1989.

Participation in Other Workshops and Meetings

– ”Computing Innovation Fellows (CIFellows) Workshop”, San Francisco, CA, May 2014.
– ”A Day at Technion”, Technion, Haifa, Israel, June 2013.
– ”30 Years of Parallel Computing at Argonne”, Argonne National Laboratory, IL, May 2013.
– ”DARPA PERFECT Program Meeting”: Arlington, VA, February 2012; Arlington, VA, July 2013; Berkeley CA, January 2014.
– ”DOE Exascale Research Conference”: San Diego, CA, March 2011; Annapolis, MD, October 2011; Portland, OR, April 2012; Portland, OR, September 2012; Berkeley, CA, March 2013.
– ”ACS Productivity Workshop”, DOD, Ford Meade, MD, July 2011.
– ”Universal Parallel Computing Research Center (UPCRC) and Illinois Intel Parallelism Center (I2PC) Summits and Workshops”: Santa Clara, CA (August 2008); Urbana, IL (February 2009); Hillsboro, OR (August 2009); Urbana, IL (March 2010); Seattle, WA (August 2010); Urbana, IL (April 2011); Santa Clara, CA (August 2011); Hillsboro, OR (December 2011); Seattle, WA (July 2012); Santa Clara, CA (August 2012); Urbana, IL (September 2013).
– ”DOE Salishan High Speed Computing Conference”, Salishan Lodge, Gleneden Beach, OR, April 2010.
– ”Google Day”, San Jose, CA, July 2008.

– ”Research@Intel Day”, Mountain View, CA, June 2008.
– ”DOE Salishan High Speed Computing Conference”, Salishan Lodge, Gleneden Beach, OR, April 2008.
– ”DOE/DOD Workshop on Emerging High Performance Architectures & Applications”, Washington, DC, November 2007.
– ”Workshop on Computer Academic/Industry Architecture Consortium (CAIAC)”, Austin, TX, September 2007.
– ”Microsoft Faculty Summit”, Redmond, WA, July 2007.
– ”DOE Salishan High Speed Computing Conference”, Salishan Lodge, Gleneden Beach, OR, April 2006.
– ”Computing Research Associtation (CRA) Conference on Grand Research Challenges: Revitalizing Computer Architecture Research”, Monterey Bay, CA, December 2005.
– ”Intel Multi-Core University Research Conference”, Portland, OR, December 2005.
– ”NSF-CISE Area Review. Area of Computer Architecture and Organization”, NSF, May 2005.
– ”DOE Salishan High Speed Computing Conference”, Salishan Lodge, Gleneden Beach, OR, April 2005.
– ”DARPA-Sponsored Information Science and Technology (ISAT) Study on Law of Large Numbers System Design”, Menlo Park, CA, February 2005.
– ”Meeting of Lead PIs of Medium and Large Projects in the Information Technology Research (ITR) NSF Program”, Washington, June 2004.
– ”DOE Salishan High Speed Computing Conference”, Salishan Lodge, Gleneden Beach, OR, April 2004.
– ”Workshop on Software for Processor-In-Memory Based Parallel Systems”, San Jose, CA, March 2004.
– ”Science Case for Large-scale Simulation,” DOE Workshop, Washington, June 2003.
– ”Review Panel of the Programa Ramon y Cajal for Returning Scientists”, Government of Spain, Madrid, June 2003.
– ”Performance Analysis and Distributed Computing (PADC 2002)”, Dagstuhl Seminar, Dagstuhl, Germany, August 2002.
– ”Performance Engineering Technology & Research Sponsored Under the NSF Next Generation Software Program”, Austin, TX, February 2002.
– ”Workshop on the Implementation of Multi-PIM Systems (WIMPS)”, Bodega Bay, CA, February 2002.
– ”Review Panel of the Programa Ramon y Cajal for Returning Scientists”, Government of Spain, Madrid, September 2001.
– ”All Hands NCSA Meeting”, Urbana, IL, May 2001.
– ”NSF-CCR Workshop on Research Directions for Next-Generation Systems Design and Integration”, Seattle, WA, June 1999.
– ”NCSA Alliance Technical Working Meeting”, Oak Brooks, IL, May 1999.
– ”The Third PetaFlop Workshop (TPF-3)”, Annapolis, MD, February 1999.
– ”IBM Workshop on Next Generation Processor Architectures”, IBM Rochester, Rochester, MN, September 1998.
– ”Petaflops Systems Operations Working Review (POWR)”, Bodega Bay, CA, June 1998.
– ”Research Workshop between the University of Illinois at Urbana-Champaign and the Centre National de la Recherche Scientifique (CNRS) of France”, Urbana, IL, April 1998.
– ”National Computational Science Alliance (NCSA) Alliance’98 Conference”, Urbana, IL, April 1998.
– ”Petaflops Algorithms Workshop (PAL’97)”, Williamsburg, VA, April 1997.
– ”Workshop on the Petaflop Frontier”, Annapolis MD, October 1996.
– ”DARPA ITO General PI Meeting”, Dallas, TX, October 1996.
– ”DARPA Workshop on Performance Evaluation”, Washington DC, September 1996.
– ”NSF Experimental Research Workshop”, Washington DC, June 1996.
– ”Petasoft: Software for Petaflop Machines”, Bodega Bay CA, June 1996.
– ”First Intel Server Forum”, Hillsboro OR, June 1996.
– ”PetaFlops Architecture Workshop PAWS’96”, Oxnard CA, April 1996
– ”1st Workshop on Computer Architecture”, Paris, France, June 1995.

Graduated 35 Ph.D. Students

1. Nima Honarmand, 2014. First Job: Assistant Professor, Department of Computer Science, Stony Brook University, Stony Brook, NY. Thesis: ”Record and Deterministic Replay of Parallel Programs on Multiprocessors”.

2. Aditya Agrawal, 2014. First Job: Member of Research Staff, NVidia, Santa Clara, CA. Thesis: ”Refresh Reduction in Dynamic Memories”.

3. Yuelu Duan, 2014. First Job: Member of Technical Staff, VMware, San Diego, CA. Thesis: "Techniques for Low Overhead Fences and Sequential Consistency Violation Recording".

4. Xuehai Qian, 2013. Current Job: Assistant Professor, Department of Electrical Engineering, University of Southern California, Los Angeles, CA. Thesis: "Scalable and Flexible Bulk Architecture".

5. Shanxiang Qi, 2013. First Job: Member of Technical Staff, Google, Mountain View, CA. Thesis: "Techniques to Detect and Avert Advanced Software Concurrency Bugs".

6. Ulya Karpuzcu, 2012. First Job: Assistant Professor, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN. Thesis: "Novel Many-Core Architectures for Energy-Efficiency".

7. Abdullah Muzahid, 2012. First Job: Assistant Professor, Department of Computer Science, University of Texas at San Antonio, San Antonio, TX. Thesis: "Effective Architectural Support For Detecting Concurrency Bugs".

8. Daniel Wonsun Ahn, 2012. Current Job: Assistant Professor, Department of Computer Science, University of Pittsburgh, Pittsburgh, PA. Thesis: "Software and Architecture Support for the BULK Multicore".

9. Pablo Montesinos, 2009. First Job: Member of Research Staff, Samsung Laboratories, San Jose, CA. Thesis: "Practical Time Travel of Multiprocessor Systems".

10. Brian Greskamp, 2009. First Job: Member of Research Staff, D. E. Shaw Research, New York, NY. Thesis: "Improving Per-Thread Performance on CMPs through Timing Speculation".

11. Radu Teodorescu, 2008. First Job: Assistant Professor, Department of Computer Science and Engineering, Ohio State University, Columbus, OH. Thesis: "Multilayer Techniques to Address Parameter Variation".

12. Abhishek Tiwari, 2008. First Job: Member of Technical Staff, Goldman Sachs, New York, NY. Thesis: "Architectural Techniques to Mitigate the Effect of Spatial and Temporal Variations in Processors".

13. Luis Ceze, 2007. First Job: Assistant Professor, Department of Computer Science and Engineering, University of Washington, Seattle, WA. Thesis: "Bulk Operation and Data Coloring for Multiprocessor Programmability".

14. James Tuck, 2007. First Job: Assistant Professor, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC. Thesis: "Efficient Support for Speculative Tasking".

15. Karin Strauss, 2007. First Job: Member of Research Staff, AMD Laboratories, Seattle, WA. Thesis: "Cache Coherence in Embedded-Ring Multiprocessors".

16. Smruti R. Sarangi, 2007. Current Job: Assistant Professor, Department of Computer Science and Engineering, Indian Institute of Technology, New Delhi, India. Thesis: "Techniques to Mitigate the Effects of Congenital Faults in Processors".

17. Jun Nakano, 2006. First Job: Member of Research Staff, IBM Research, Tokyo, Japan. Thesis: "Techniques to Address Unreliability and Variability of Computing Systems".

18. Jose Renau, 2004. First Job: Assistant Professor, Department of Computer Engineering, University of California, Santa Cruz. Thesis: "Chip Multiprocessors with Speculative Multithreading: Design for Performance and Energy Efficiency".

19. Milos Prvulovic, 2003. First Job: Assistant Professor, College of Computing, Georgia Institute of Technology, Atlanta, GA. Thesis: "Architectural Support for Reliable Parallel Computing".

20. Jose Martinez, 2002. First Job: Assistant Professor, Department of Electrical and Computer Engineering, Cornell University, Ithaca, NY. Thesis: "Speculative Shared-Memory Architectures".

21. Yan Solihin, 2002. First Job: Assistant Professor, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC. Thesis: "Improving Memory Performance Using Intelligent Memory".

22. Michael Huang, 2002. First Job: Assistant Professor, Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY. Thesis: "Managing Processor Adaptation for Energy Reduction and Temperature Control".

23. Anthony Nguyen, 2002. Current Job: Member of Research Staff, Intel Corporation, Santa Clara, CA. Thesis: "High-Throughput Coherence Controllers".

24. Marcelo Cintra, 2001. First Job: Lecturer, School of Informatics, University of Edinburgh, UK. Thesis: "Architectural Support for Scalable Speculative Parallelization in Shared-Memory Multiprocessors".

25. Seung-Moon Yoo, 2001. First Job: Member of Research Staff, IBM Research, Austin, TX. Thesis: "Design of Energy-Efficient SOCs with Deep Sub-Micron Circuit Techniques".

26. Qiang Cao, 2000. First Job: Member of Technical Staff, Oracle Corporation, Redwood Shores, CA. Thesis: "Performance Characterization and Buffer Memory Optimization of Databases".

27. Sujoy Basu, 2000. First Job: Member of Research Staff, Hewlett-Packard Laboratories, Palo Alto, CA. Thesis: "Design of Efficient Simple COMA Architectures".

28. Yi Kang, 1999. First Job: Microprocessor Design Group, Sun Microsystems, Menlo Park, CA. Thesis: "An Intelligent Memory for Data Intensive Applications".

29. Ye Zhang, 1999. First Job: Member of Technical Staff, Oracle Corporation, Redwood Shores, CA. Thesis: "Speculative Parallelization in DSM Multiprocessors".

30. Pedro Trancoso, 1998. Current Job: Lecturer, Department of Computer Science, University of Cyprus, Cyprus. Thesis: "Optimizing Memory-Resident DSS Workloads for Caches".

31. Venkata Krishnan, 1998. First Job: Microprocessor Design Group, DEC Shrewsbury, MA. Thesis: "Speculative Multithreading Architectures".

32. Liuxi Yang, 1997. First Job: Microprocessor Design Group, Sun Microsystems, Menlo Park, CA. Thesis: "Using Advanced Memory Technologies to Build DSM Multiprocessors".

33. David Koufaty, 1997. First Job: Member of Technical Staff, Intel Corp, Hillsboro, OR. Thesis: "Compiler Support to Hide Coherence Misses in Shared-Memory Multiprocessors".

34. Zheng Zhang, 1996. First Job: Member of Research Staff, Hewlett-Packard Laboratories, Palo Alto, CA. Thesis: "Design Alternatives to Reduce Remote Conflict Misses in Shared-Memory Multiprocessors".

35. Chun Xia, 1996. First Job: Member of Technical Staff, Sun Microsystems, Menlo Park, CA. Thesis: "Exploiting Multiprocessor Memory Hierarchies for Operating Systems".

Graduated M.S. Students

- Russell Daigle, Xiangfeng Chen, David Oesterreich, Alain Raynaud, Kittipong Mungnirun, Pedro Trancoso, Arun Sharma, Jovan Mitrevski, Jose Martinez, Zhenzhou Ge, Michael Huang, Yan Solihin, Jose Renau, Milos Prvulovic, Vinh Lam, James Tuck, Kuan Chen, Smruti Sarangi, Radu Teodorescu, Paul Sack, Brian Greskamp, Pablo Montesinos, Abdullah Muzahid, Ulya Karpuzcu, Shanxiang Qi, Rishi Agarwal, Marios Nicolaides, Ben Ahrens, Raghavendra Pothukuchi.

Postdoctoral Researchers

1. Sanyam Mehta, October 2014 - pres., from University of Minnesota.

2. Wonsun Ahn, Apr 2012 - Aug 2014, from University of Illinois.

3. Amin Ansari, Sep 2011 - Aug 2013, from University of Michigan.

4. Wei Liu, Aug 2001 - Aug 2006, from Tsinghua University, China; Now at Intel Corp.

5. Basilio Fraguela, Aug 2001 - Aug 2002, from Universidade A Coruna, Spain.

Visiting Scientists

1. Oscar Plata, Sep 2015 - Nov 2015, Universidad de Malaga, Spain.
2. Sonia Gonzalez, Sep 2015 - Nov 2015, Universidad de Malaga, Spain.
3. Sergi Abadal, May 2015 - Nov 2015, Universitat Politecnica de Catalunya, Spain.
4. Benjamin Sanhelices, Aug 2010 - Dec 2010, Universidad de Valladolid, Spain.
5. Lois Orosa, Sep 2009 - Dec 2009, Universidad de Santiago, Spain.
6. Norimasa Otsuki, Aug 2009 - Aug 2010, Renesas Technology, Japan.
7. Dario Suarez, May 2008 - Jul 2008, Universidad de Zaragoza, Spain.
8. Daniel Chaver, Jul 2002 - Aug 2002, Universidad Complutense de Madrid, Spain.
9. Keiji Kimura, Aug 2001 - Oct 2001, Waseda University, Japan.
10. Pedro Trancoso, Jul 2000 - Aug 2000, International College, Limassol, Cyprus.
11. Jaejin Lee, Aug 1999 - Dec 1999, Michigan State University, MI.
12. Paul Feautrier, Feb 1999 - May 1999, Universite de Versailles, Versailles, France.
13. Diego Llanos, May 1999 - Jul 1999, Universidad de Valladolid, Valladolid, Spain.
14. Josep Lluis Larriba-Pey, Apr 1996 - Sep 1996 and Jul 1997 - Sep 1997, Universitat Politecnica de Catalunya, Barcelona, Spain.

Teaching Activity

- Extensive teaching and advising experience at the undergraduate and graduate levels. Taught undergraduate- and graduate-level courses on computer architecture, computer organization, and logic design at UIUC.
- Was invited to talk about "Computer Architecture Education at the University of Illinois" at the 2nd, 4th, and 5th Workshop on Computer Architecture Education, February 1996, January 1998, and June 1998.
- Appeared several times in the local student newspaper Daily Illini under "Incomplete List of Teachers Ranked Excellent By Their Students".
- Some of the courses taught were broadcasted to large off-campus audiences, both in the U.S. and in India.
- Organized the weekly Illinois-Intel Parallelism Center (I2PC) Distinguished Speaker Seminar (August 2011 - August 2013), and invited many Intel personnel to speak.
- Created a graduate-level weekly research seminar: "Research Topics in Advanced Computer Architecture".
- Developed semester-long special-topics courses: "Shared-Memory Multiprocessors: Architecture and Programming" (Spring 93) and "Research Issues in New Processor and Memory Architectures" (Spring 01).

Other Major Service Outside UIUC

- Participant in many NSF and DARPA workshops, PI meetings, and program-conception meetings, including DARPA's "Data Intensive Systems", "Bio-Computation", "Polymorphous Computer Architectures", "High Productivity Computer Architectures", "Ubiquitous High Performance Computing", and "Power Efficiency Revolution for Embedded Computing Technology".
- Presented the outcome of Computing Community Consortium workshops to CCC, DOE, NSF, AFOSR, and NITRD.
- CCC-appointed liaison to guide the visioning workshops on "Charting the Future of Electronic Design Automation", March 2013, June 2013, and February 2014.

- Member of the Steering Committee, IEEE Computer Society Multicore, April 2013 - pres.
- Member of the IEEE Fellows Selection Committee, 2012-2013.
- Member, Computing Innovation Fellows Selection Committee, CCC and CRA, 2010.
- Member, Search Committee for Editor-in-Chief of the Computer Architecture Letters (CAL) journal, 2005.
- Member of the Advisory Board, Department of Electrical and Computer Engineering, University of Rochester, 2003-pres.
- Member of Enabling Technologies Team A, NSF's National Computational Science Alliance (NCSA) Partnership for an Advanced Computational Infrastructure (PACI), 1997 - 2004.
- I-ACOMA research project was selected as one of the "Eight Point-Design Studies" that DARPA, NSF, NSA and NASA supported in 1996, in a nationwide effort to accelerate the arrival of a petaflop-level machine.
- Participant in many NSF Proposal Evaluation Panels: March 1996, November 1998, March 2000, July 2001, February 2002, February 2003, May 2004, August 2004, October 2007, April 2008, December 2008, April 2009, March 2010, December 2010, March 2011, March 2012, May 2013, June 2014.
- Regular referee for the major conferences and journals in computer architecture and parallel processing, and reviewer of books on computer architecture.

Major Service Inside UIUC

- Member of College of Engineering Executive Committee (2002-2008) and Grievance Committee.
- Served in many committees at the College of Engineering and at the Department of Computer Science.
- Member, Computer Science Department Head Review Committee, 2015.
- Chair, Architecture and Hardware Area, Department of Computer Science, 2004-2006.
- Member, Parallel Computing Institute (PCI) Growth Committee, 2013-pres.
- Host to many speakers and visitors invited to the Department of Computer Science.
- Participated and organized faculty retreats for the Computer Science Department, Computer Engineering, and College of Engineering.
- Participated in several Illinois Computer Science Alumni reunions across the nation.

Other Activities

- Consultant for several companies.
- Consultant for patent assessment. Member of the Round Table Group (RTG) Network of Patent Consultants.