EXTREME SCALE DESIGN AUTOMATION

CCC/SIGDA Workshop Series

Alex K. Jones
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Classic Moore's Law:
Made New Designs Possible, Old Ones Lucrative

- Silicon Process Technology
- Intel 386™ DX Processor
- Intel 486™ DX Processor
- Pentium® Processor
- Pentium® II, III Processors
- Pentium® 4

30 engineers, ½ yr
Cheap, fast, easy profitable proliferations
Source: Bob Colwell
Intel, DARPA

500+ engineers, 5 years
Big, hot, expensive, risky flagships
SURVEY: WILL MOORE’S LAW END?

- Traditional (Dennard) scaling ended 10 years ago (sub 80nm)
- Industry roadmap will continue to find patches to silicon (5nm)
  - Seems the cost scaling proposition may have ended

EDA is still chasing a *multi-dimensional* moving target

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4225 survey takers responded to this question

- It’s dead now: 19.64% (830)
- Yes, at 28nm: 4.64% (196)
- Yes, at 14nm: 9.61% (406)
- Yes, at 7nm: 10.53% (445)
- Yes, at 5nm: 11.34% (479)
- No, graphene will keep it alive: 12.66% (535)
- No, 3D stacks will extend it: 14.34% (608)
- No, it will never end: 13.68% (578)
- Other (specify in the comments below): 3.55% (150)

Source: EE Times Survey
March 2014
EXTREME SCALE SILICON ROADMAP

EUV Saves Costs versus Double Patterning

450mm Increases Throughput to Save Cost

What is clear?
EDA will become increasingly important at the Extreme Scale

Will scale to 10nm? 7nm? 5nm?

FD-SOI?
All around gate transistors?
CCC/SIGDA WORKSHOPS ON EXTREME SCALE DESIGN AUTOMATION

Series of three workshops:

• Workshop 1: **Emerging Technologies and Workforce Continuity**
  – March 7-8, 2013 Pittsburgh

• Workshop 2: **Extreme Scale Chips and Industry Research**
  – June 2-3, 2013 Austin (Collocated with DAC)

• Workshop 3: **Achieving Sustainable Collaborations Through Abstractions, Methodologies, and Benchmarks**
  – February 20-21, 2014 Tampa

The purpose of this workshop series was to take an introspective look at the EDA field while crystalizing a vision for both the near and long term.
WHERE SHOULD EDA INVEST?

Major Focus Areas

• Extreme-scale Electronic Design Automation (ESDA)
  – First *Big Data* Discipline, $10^{15}$ devices
  – Focus on *System-level Design* and *Verification*

• Emerging Technologies (Post-CMOS/Hybrid)
  – Develop Full System Flows
  – Technology choices: more than *ad hoc* demonstrations

• New Markets (DAoT)
  – Near term: CPS/IoT, Cyber-secure systems (hardware)
  – Medium term: Biology/Medical Technology

• Cross Cutting
  – Abstractions, Metrics, Benchmarks
  – Synergy with Computer Architecture
  – Education and Workforce
EXTREME SCALE DESIGN AUTOMATION

Continuing Onward: Next-Generation Electronic Systems
ESDA IS AN EXCITING TIME FOR EDA

EDA's Objectives “at a glance”

ITRS Productivity Curve


Time

Technology Capabilities
2x/36 months

HW Design Productivity
Filling with IP and Memory

HW Design Gap

Log

Gates/Chip

Gates/Day

Figure 1: The design productivity gap

Level of Abstraction

Quality

(result = QOR; PPAY=

power, performance, area and yield

Paradigm
domain-specific,
stochastic and approximate
computing, etc

Application

Time-scale of the
research lifecycle in years

How are we doing?

This uncertain, and exciting environment is reminiscent of the beginnings of the EDA era prior to the stability provided by Dennard scaling.

Uncertainty of the current environment is alleviated by the large global demand for IC products

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WHAT ABOUT “LEGACY” TECHNOLOGY NODES?

130nm design starts dominate the market

Barriers
- “Good enough solutions”
- Fear new methods break tools
  - Unintended side effects
- Push button flows still achievable
  - Inadequate investment

130nm designs are popular
- Reduces upfront cost
- Increases yield

Closing the productivity gap at 130nm could approximate current technology capabilities

An EDA advancement demonstrated in a tool that finds superior solutions is particularly valuable to effectively utilize legacy technology nodes.
HYBRID POST-CMOS ELECTRONICS

ROLE OF EMERGING TECHNOLOGIES

Replace Si-CMOS?

- There are many emerging technologies
  - Most are niche
  - Likely hybrid solutions

Challenges

- Integration
- Stochastic behavior
- Models and abstractions
- Full system demonstrations

EDA should not determine which new technologies to pursue.
EDA should address new technology specific challenges for EDA flows.

<table>
<thead>
<tr>
<th>TECHNOLOGY</th>
<th>PROPOSED USE</th>
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<tbody>
<tr>
<td>Optical interconnect, optical devices</td>
<td>High-performance, high-bandwidth communications</td>
</tr>
<tr>
<td>Terahertz (RF) circuits</td>
<td>Automotive radar, security, high-bandwidth wireless communication</td>
</tr>
<tr>
<td>Phase-change memories (including memristors)</td>
<td>DNA memory (having long retention)</td>
</tr>
<tr>
<td>Microfluidics</td>
<td>Lab-on-a-chip, cooling</td>
</tr>
<tr>
<td>Steep slope devices</td>
<td>Ultra low-power computing</td>
</tr>
<tr>
<td>Superconductors</td>
<td>Ultra low-power computing, ultra high performance</td>
</tr>
<tr>
<td>Carbon-based electronics</td>
<td>Ultra low-power computing, high performance, monolithic 3D ICs</td>
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</tbody>
</table>

Figure 4: Emerging technologies for the EDA community.
THE HYPE CYCLE OF INNOVATION

Generalized Pattern of Research and Commercialization
From Conception to Productive Use

- Mass media: Hype begins
- First-generation products, price, lots of customization needed
- Second-generation products developing
- Third-generation products, some services

EDA Minimizes the Trough of Disillusionment
EDA Maximizes the Slope of Enlightenment

High-growth adoption phase starts: 20 to 30 percent adoption

NSF NEB Program–EDA should be included

EDA Can Lead to Concrete Evaluation of New Technologies
THE DESIGN AUTOMATION OF THINGS

Looking Forward: New Markets and Applications
THE POWER OF DESIGN AUTOMATION

Success of Electronic DA

- Facilitated unprecedented exponential advancement of Si/CMOS
- EDA separates
  - Design
  - Construction
  - Optimization

- Clear abstraction & predictive models of low-level behavior allows:
  - High level analysis
  - Optimization
  - Verification

DA Techniques Beneficial to Areas

- Require analysis before construction
- Lack appropriate abstractions
- Rely on both optimization and analysis to meet specs
- Can make low cost alternatives to high cost products
- Need efficient assessment of outcomes prior to construction

- Biological and Medical Technologies
- Cyber-physical Systems
- Cyber-secure Systems
NEW MARKETS WHERE DESIGN AUTOMATION CAN BE TRANSFERRED

**NSF CPS–EDA** identified but missing

**NSF STARSS–EDA** also missing

**NSF EFRI–BioDA** potential topic
CROSS CUTTING CHALLENGES

Abstractions, Metrics, and Benchmarks
Education and Workforce
Synergies with Computer Architecture
EDUCATING IN EDA

“EDA? But I want to do something cool!”

“EDA? But I want to save the planet!”

• Students want to impact society
• EDA is not perceived to “change the world”

• EDA is TWO levels of indirection away from “cool”

“What do you mean, build the tools that make the chips that make the smartphone? Can’t I just write apps for Google?”

Industry University Partnerships!

Activity creates excitement
CURRICULUM AND STRATEGY

• I teach the same old courses the same way, it works!
• Students can't learn this stuff before they know "the basics"
• Students will see the importance of MY course
• We should call the course what it is: "formal methods"

Better marketing to students

Make EDA fun (e.g., Crowdsourcing)

Critical Mass & MOOCs
CONCLUSIONS
### Dimensions of Future EDA Activities

<table>
<thead>
<tr>
<th>Electronics: Hybrid CMOS with Emerging Technologies</th>
<th>New Markets: Cyber-physical, Cyber-secure, and Bio-medical Technologies</th>
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<tbody>
<tr>
<td><strong>Traditional EDA Tool-kit</strong></td>
<td>Immediate Need: EDA for scaled CMOS + product ready tech</td>
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<td></td>
<td>Immediate Need: EDA applied to near fields – automotive, robotics, and energy</td>
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<tr>
<td><strong>EDA Approaches on Big Data</strong></td>
<td>Transformative: Big data research–system level design and verification</td>
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PARTICIPANTS AND CONTRIBUTORS

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Workshops on Extreme Scale Design Automation (ESDA) Challenges and Opportunities for 2025 and Beyond

R. Iris Bahar, Alex K. Jones, Srinivas Katkoori, Patrick H. Madden, Diana Marculescu, and Igor L. Markov

Abstract

Integrated circuits and electronic systems, as well as design technologies, are evolving at a great rate—both quantitatively and qualitatively. Major developments include new interconnects and switching devices with atomic-scale uncertainty, the depth and scale of on-chip integration, electronic system-level integration, the increasing significance of software, as well as more effective means of design entry, compilation, algorithmic optimization, numerical simulation, pre- and post-silicon design validation, and chip test. Application targets and key markets are also shifting substantially from desktop CPUs to mobile platforms to an Internet-of-Things infrastructure. In light of these changes in electronic design contexts and given EDA’s significant dependence on such context, the EDA community must adapt to these changes and focus on the opportunities for research and commercial success. The CCC workshop series on Extreme-Scale Design Automation, organized with the support of ACM SIGDA, studied challenges faced by the EDA community as well as new and exciting opportunities currently available. This document represents a summary of the findings from these meetings.

For more information
http://www.cra.orgccc/visioning/visioning-activities/esda
THANK YOU!

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