

Proposal Example 3

Visioning Topic Area

Computing systems, though pervasive in society, are as yet unable to demonstrate the energy efficiency of the human brain, especially in tasks requiring cognition, inference, and decision-making. Indeed, the most computationally-challenging emerging applications today involve some form of information extraction from available data. Information extraction is a computationally intensive process consuming substantial energy implemented on conventional von Neumann processors. Traditionally, computing systems have relied on scaling of transistor feature sizes for enhancing energy efficiency, throughput, performance, functional density, and most importantly cost (per component). Dennard scaling of feature sizes is has slowed down. Many factors have contributed to this slow down, not the least of which is the emergence of stochastic behavior, intrinsic in emerging nanofabrics – a behavior that is completely at odds with the requirement of an ideal deterministic switch imposed by the von Neumann architecture.

Future computing systems need to overcome the fundamental efficiency-robustness barrier in order to continue to have societal-scale impact. A key requirement is to envision this future as a convergence of three focus areas – ***emerging inference applications, beyond CMOS nanofabrics, and alternative models and architectures for computing***. The proposed workshop is organized around these three focus areas.

A compelling vision of future computing systems would be one where the *statistical application metrics* in the inference space are accounted for during design, where unique statistical attributes of nanoscale fabrics would be exploited for designing *stochastic nanofunctions* required by these applications, and where alternative models for computing and *statistical information processing* would be leveraged to design systems meeting application-level requirements. Achieving this vision calls for a journey from systems-to-nanofabrics and back. This journey has been undertaken since 2013 by some of us as part of the SONIC (Systems on Nanoscale Information fabriCs) Center (<http://www.sonic-center.org>). This 1-day workshop will bring together a broad community of leading researchers from the areas of nanoscience, neuroscience, architecture, integrated circuits and nanodevices, to brainstorm on ideas for designing information processing platforms of the future on beyond CMOS nanoscale process technologies that approach the energy efficiency and the decision-making functionality of the human brain.

Proposed Activities

The workshop will be organized along the three focus areas - *emerging inference applications, beyond CMOS nanofabrics, and alternative models and architectures for computing*.

The workshop will be preceded by a number of pre-workshop preparatory activities in order to enhance the productivity on the day of the workshop. These are in addition to the standard workshop logistics. These activities will be based around the working group structure. All workshop participants will be

members of a working group. Each working group will be expected to engage in preliminary discussions and research prior to the workshop. The pre-workshop activities are outlined below with tentative time lines (indicates completion date):

1. **Formation of working groups (3 months prior):** the invitations sent to attendees will include a requirement that they agree to participate in a specific working group. There will be 1 to 2 working groups per area so as to keep the number of members per working group reasonable in size. Each working group will have a chair who will be responsible for coordinating the activities of the working group.
2. **Providing a charter to each working group (2 months prior):** Each working group will be provided with a survey whose answers would need to be obtained via discussions between the working group members. These questions will focus on obtaining relevant data and suggesting topics for preliminary discussions. In addition, the working groups will be asked to upload key, supporting publications onto a shared workshop folder.
3. **Working group deliverables (2 weeks prior):** Each working group will provide responses to the survey to the organizing committee, and would have uploaded key, supporting publications on to the shared folder. The answers from all working groups will be compiled and shared with all attendees on the day of the workshop.

The workshop format will be structured to cross-fertilize the three focus areas. A tentative workshop agenda is as follows:

1. **AM:** Introductory remarks by workshop organizers, followed by presentations by working group chairs. The working group chairs will ensure that both consensus and dissenting opinions are presented.
2. **PM:** Parallel break-out sessions will be organized. Each session will involve members from all three areas focusing on a specific topic. Session chairs will be appointed to moderate the discussions and summarize the findings.
3. **Conclusion:** the meeting will conclude with a panel comprising session and working group chairs.

Justification of Workshop Timeliness

On 20th October 2015 the White House Office of Science and Technology Policy (OSTP) (<https://www.whitehouse.gov/blog/2015/10/15/nanotechnology-inspired-grand-challenge-future-computing>) announced a Nanotechnology-inspired Grand Challenge for Future Computing. It states “.... *current technology falls far short of the human brain in terms of both the **brain’s sensing and problem-solving abilities** and its **low power consumption** fundamental physical limitations will prevent transistor technology from ever matching these twin characteristics. We are therefore challenging the nanotechnology and computer science communities to look beyond the decades-old approach to computing based on the Von Neumann architecture as implemented with transistor-based processors, and chart a new path that will continue the rapid pace of innovation beyond the next decade.....To meet*

*this challenge, **major breakthroughs are needed** not only **in the basic devices** that store and process information and the amount of energy they require, but **in the way a computer analyzes images, sounds, and patterns; interprets and learns from data; and identifies and solves problems.***

Some of the organizing committee of the proposed workshop, are members of the Systems on Nanoscale Information fabriCs (SONIC), a multi-university research center funded by the Semiconductor Research Corporation and DARPA under the STARnet program since 2013. The STARnet program is referred to in the OSTP announcement as one where initial advances on this topic are being made. In SONIC, researchers from nanoscience, neuroscience, architecture, integrated circuits, have already been collaborating to develop Shannon (information theory) and brain-inspired models of statistical information processing algorithms, architectures, and integrated circuits prototypes on scaled CMOS and beyond CMOS nanofabrics. This workshop will leverage the research results of SONIC to engage a broad cross-section of researchers from the areas of computing, nanoscience, neuroscience, architectures and integrated circuits, in order to identify promising research directions that will help to achieve the goals set by the OSTP Grand Challenge.

Workshop Outcomes

This workshop will result in a written report describing specific recommendations for new research directions that will be shared with a number of federal agencies. A set of slides presented at the workshop will be attached in the appendix to this report.

Organizing Committee Members

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Representative List of Workshop Invitees

The following is a representative list of workshop invitees. This list is subject to change based on availability of speakers and inclusion of additional names in the list. We expect a vast majority of the attendees to participate actively in presentations and/or discussions.

- **EMERGING INFERENCE APPLICATIONS AND ALGORITHMS: ...**
- **BEYOND CMOS NANOFABRICS AND CIRCUITS:...**
- **Alternative models and architectures for computing: ...**

Budget

Funds to support a workshop with 20-30 attendees will be requested.

Metrics of Evaluation

The success of the workshop will be evaluated in terms of the number and size of new research programs connecting nano and system sciences for the purpose outlined in the OSTP Grand Challenge. Another metric will be follow-on meetings and workshops co-located with major conferences in computing and nanotechnology.