Path to Widespread Adoption of Reversible Classical/Adiabatic Logic Technology by Industry

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Outline

- Goal
  - Widespread adoption of reversible logic
  - Meeting AF Needs
- Timeline of Air Force Efforts
  - Energy Consequences of Information Workshop
  - STTR Phase 1
  - STTR Phase 2
- Growing Interest/Demonstrating Benefits
  - Other demonstrations comparing conventional and adiabatic
  - What is the best way to compare implementations?
- Requirements
  - Improving tools
  - Killer applications

USAF/USSF Interest in Reversible/Adiabatic Approaches

- Meeting Air Force/Space Force Needs
  - Processing requirements of future space systems growing rapidly – need to get <u>better</u> data products to the warfighter <u>faster</u>, manage <u>larger</u> numbers of satellites from the theater
    - Autonomous operation – simplified mission planning, response to environmental threats
    - Image processing - larger formats and higher frame rates - driving processors & memory
  - Resource constraints – drive size, weight and power demands on a satellite
    - Available energy (Energy from solar panels ~ area), Heat dissipation ~ area * T^4
    - Limits power use by microprocessors → limits capability
    - Additional Constraints Imposed by Space Environment
      - Mission Reliability - 2-15 year lifetime on orbit? Depends on orbit
      - Radiation Tolerance – Depends on orbit
      - Impact of reversible computing unknown, but not expected to differ from traditional approaches
  - Cost
    - Chip design & fabrication costs for large scale processors have grown rapidly over time – government cannot go it alone
    - <u>Need to leverage both government and industry interest and investment</u>

Our challenge – attract sufficient interest from all parties to garner needed investments and technology developments

History of AF Efforts

- Energy Consequences Of Information Workshop – February 2017, Santa Fe, NM
  - AFRL, DoE, AFOSR
  - Cast a broad net looking at approaches to energy efficient computing in multiple domains, satellites to supercomputers
  - Inspiration for new research areas in our program – In-house and SBIR/STTR calls
- STTR Topic AF18B- T013 to develop and characterize a test chip implementing adiabatic/reversible logic side-by side with conventional logic implementation
  - Compare performance while controlling for other factors such as process technology, etc.
- Two teams selected for Phase 1 Chip Design Study (December 2018-September 2019)
  - Indiana Integrated Circuits/Notre Dame – focused on 1 logic approach and proposed reduced instruction set microprocessor @ 500 MHz that could be operated in both reversible and conventional modes
  - Signal Solutions/University of Kentucky – proposed a study of multiple adiabatic logic approaches using simpler circuits
  - Both studies provided valuable insights – would have liked to fund both for phase 2
- IIC/ND selected for Phase 2 – fabricate and test their design
  - Delayed start due to changes in the AF SBIR/STTR program, awarded in 2nd quarter of 2020
  - Hoping to have silicon around 2nd quarter of 2021
  - See IIC/ND team presentation for details

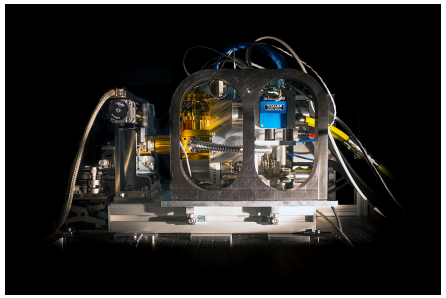
What should be next?

Questions on Growing Interest/Demonstrating Benefit

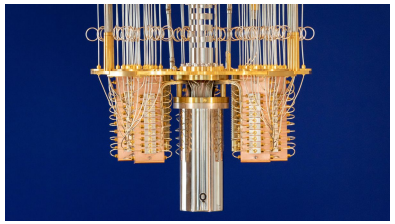
- IIC/ND program is attracting both government and commercial interest, so what should our strategy be going forward? Some questions to consider:
  - Do we have the right approach to garner long term interest?
    - May not convince customers, competing against 50+ years of design strategy
    - Our comparison, while necessary, is somewhat constrained
      - In the end need to demonstrate that this leads to a better solution
        - Need to compare an optimal conventional solution against an optimal adiabatic solution
    - We expect the current apples-to-apples comparison to show a 1-2 order of magnitude energy benefit
      - If the approach scales to more complex designs, this may be enough

Questions on Growing Interest/Demonstrating Benefit

- Do we have the right application?
  - Memory logic – much of the operating cost of HPC systems is energy dissipated by RAM – suggests a place in the memory hierarchy of a computer system
  - Readout logic for cryogenic sensors – does not need GHz operating speeds and adiabatic logic works best @ MHz where energy reductions are O(10^6)
  - Control logic for quantum computing – since most dissipation is in the clocks, dissipation can be moved out of the cold bath



RAPID IR Sensor, Precision Integrated-Optics Near-Infrared Imaging Experiment (PIONIER), European Southern Observatory (Paranal Observatory) By ESO - http://www.eso.org/public/images/ann15042a/, CC BY 4.0, https://commons.wikimedia.org/w/index.php?curid=40978824



IBM Quantum Computer

- Do we have the right adiabatic logic type? Is there a one size fits all approach that can work?
- What energy reduction strategies can we leverage from commercial technology – e.g., multi-core, dark silicon?

Things we probably need to go forward

- Tools and libraries developed for optimized, adiabatic logic design of complex circuits - need to manage complexity of logic and timing on large scales
- Applications that will attract broad interest and funding
  - Internet of Things
  - Ultra-low power memory
- Continued work on competing classes of adiabatic logic

Open for Discussion

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