



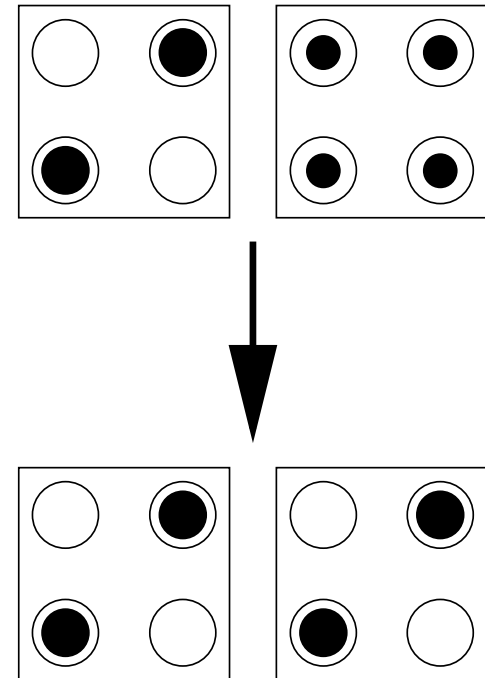
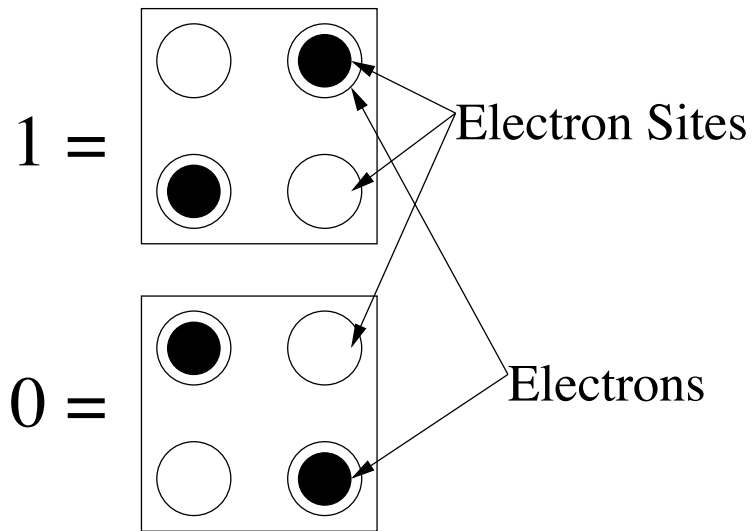
Gem State
INFORMATICS

Quantum-dot Cellular Automata: A Brief Introduction Sarah Frost-Murphy

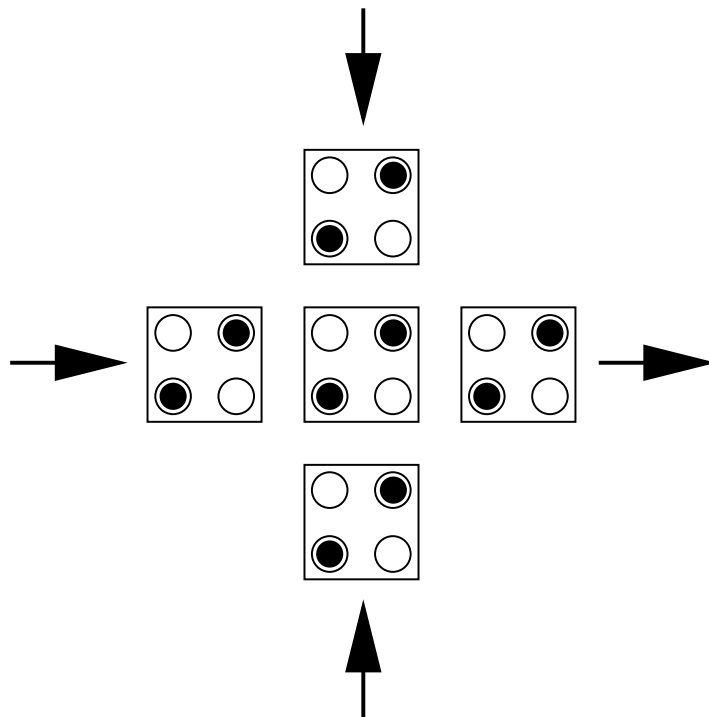
Overview

- Basic Device Operation
- Faults and Fault Tolerance
- The Clock
- Real QCA devices
- Architecture: Proof of Concept
- Floorplans
- Reversibility with QCA

The Basic Device



Majority Gate

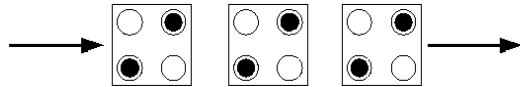


A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Fixed "0" Input

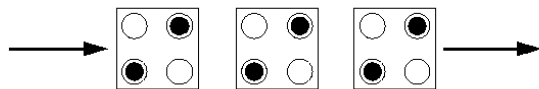


Majority Gate



AND

Fixed "1" Input

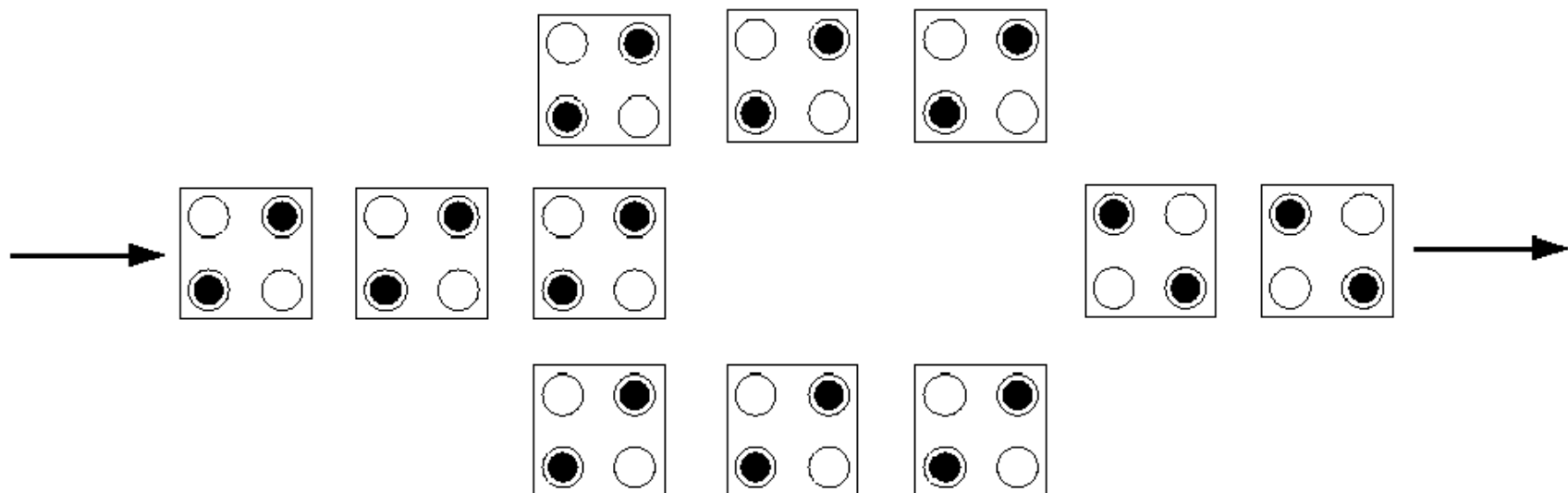


OR

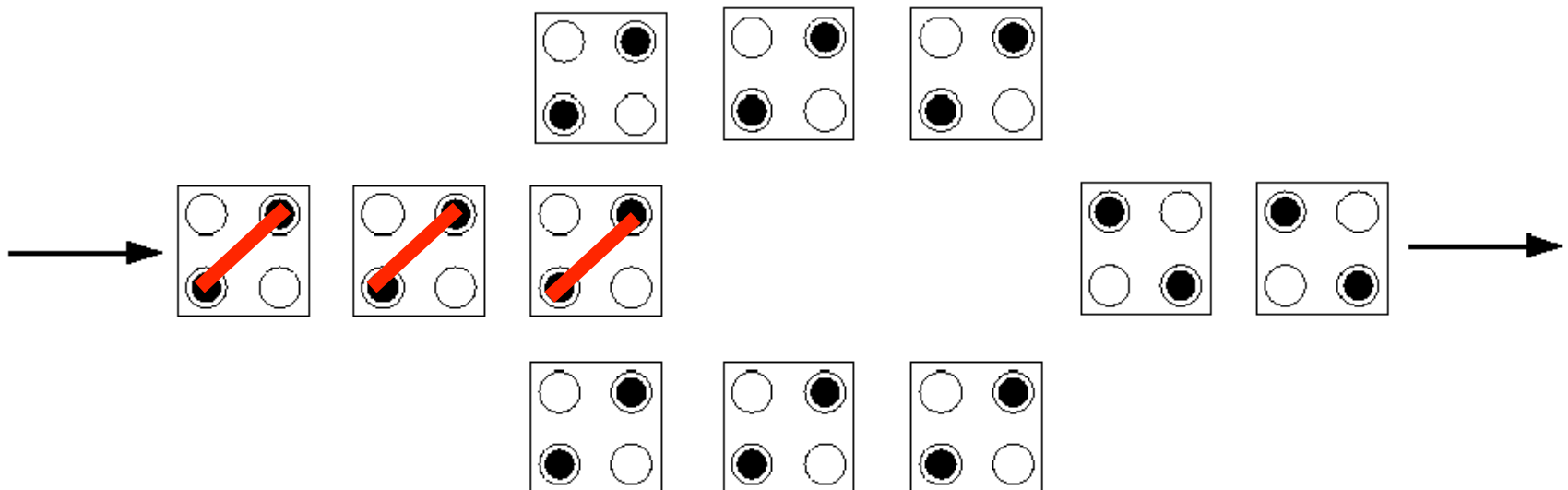
(d)

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

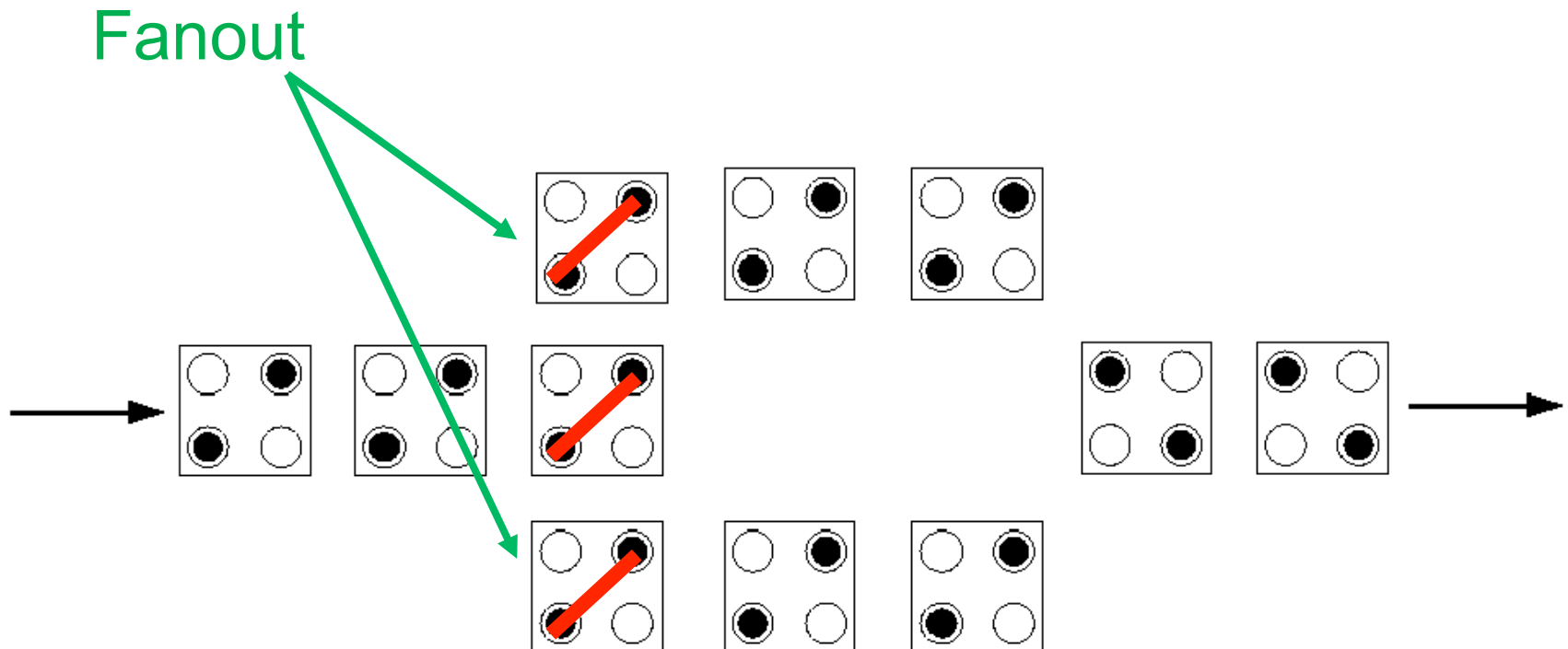
NOT Gate



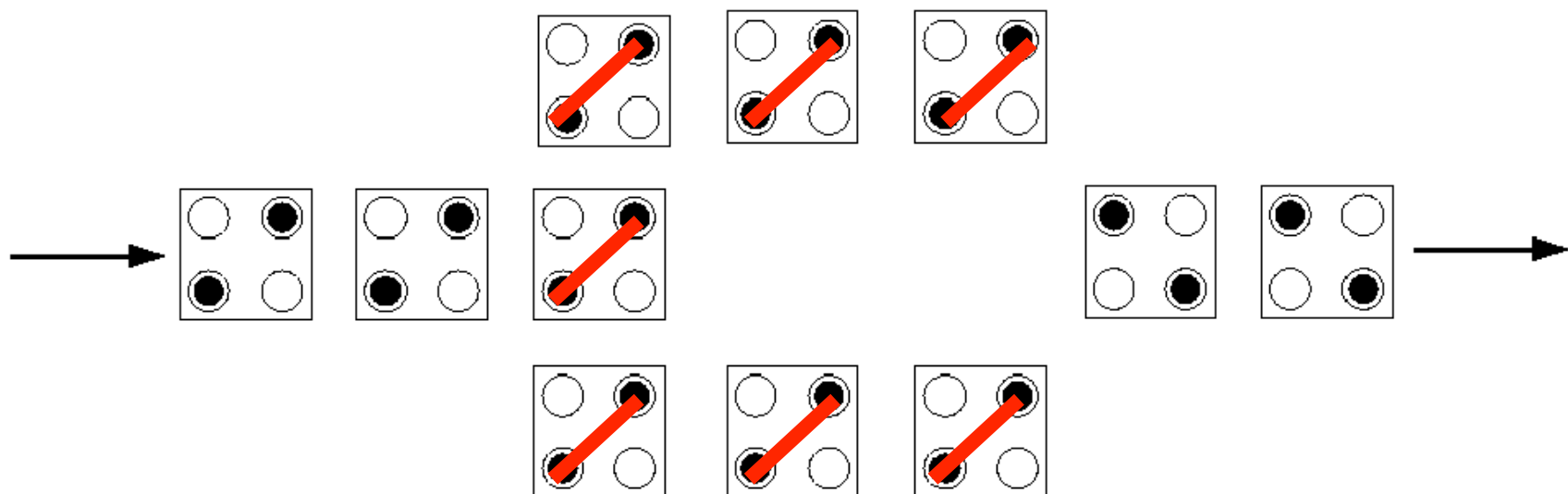
NOT Gate



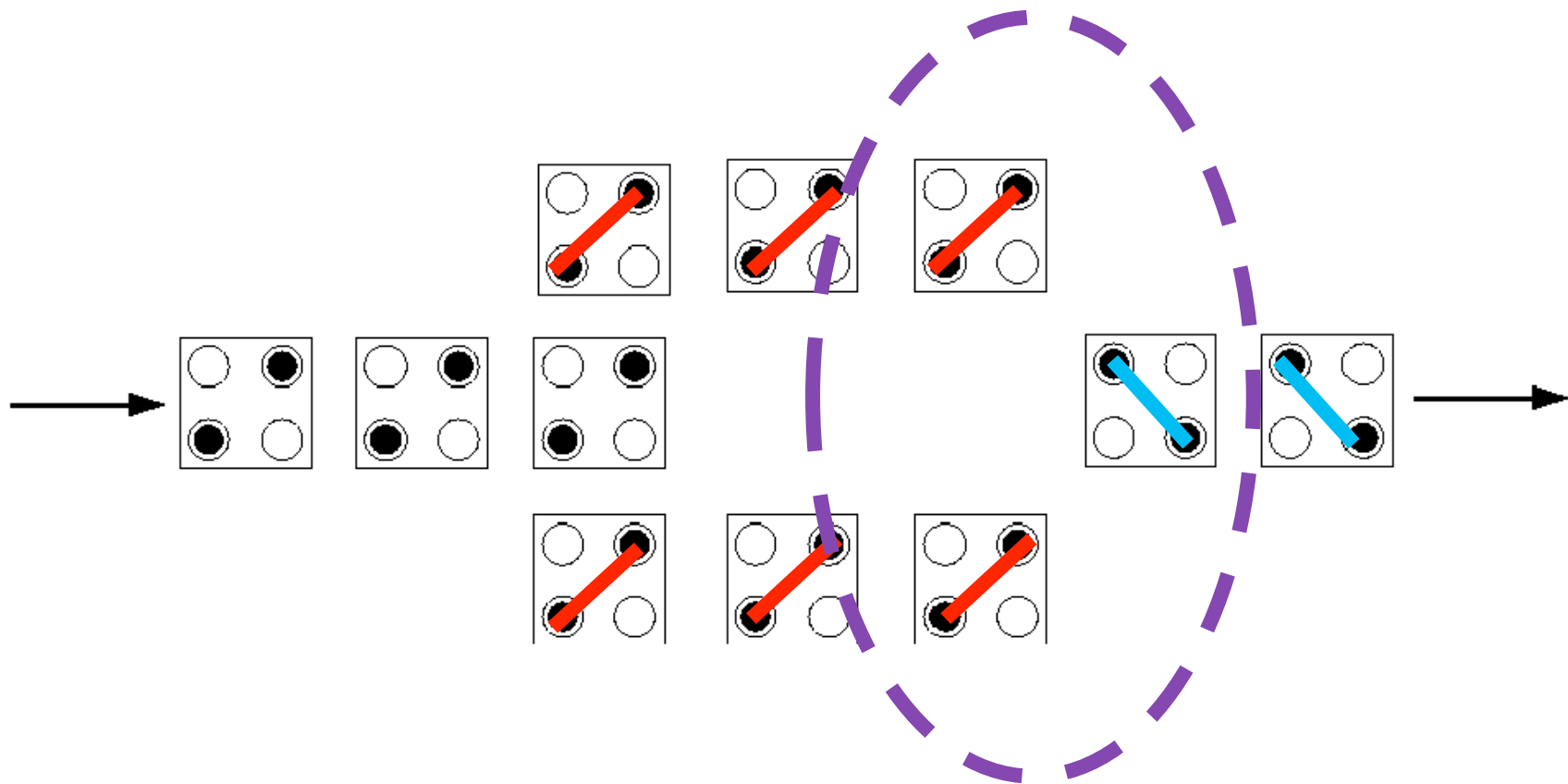
NOT Gate



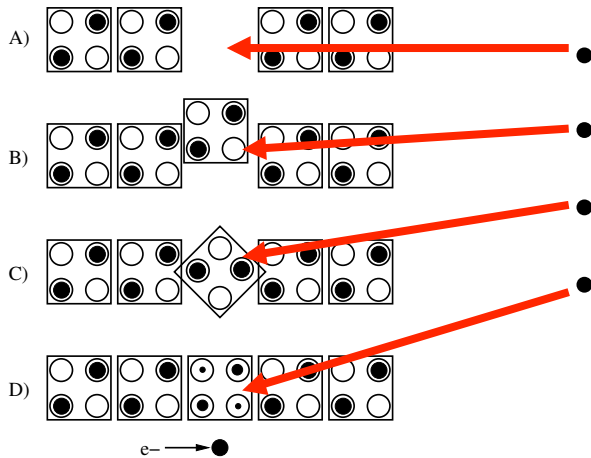
NOT Gate



NOT Gate

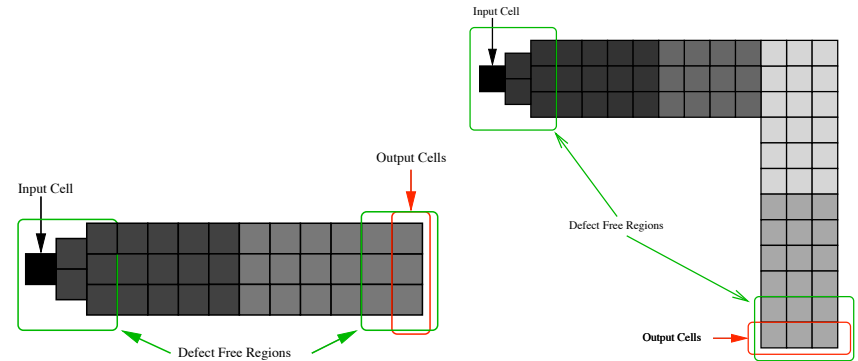


Fault Tolerance



Dysart, 2009

- Missing cell defect
- Displacement defect
- Rotation defect
- Stray charge defect

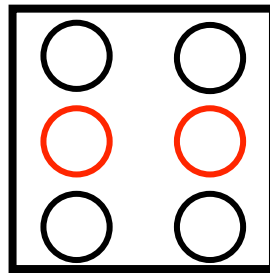
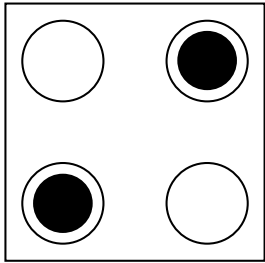


(a) A 3-wide straight wire.

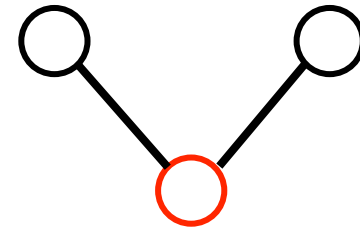
(b) A 3-wide bent wire.

Dysart, 2005

Clocked QCA

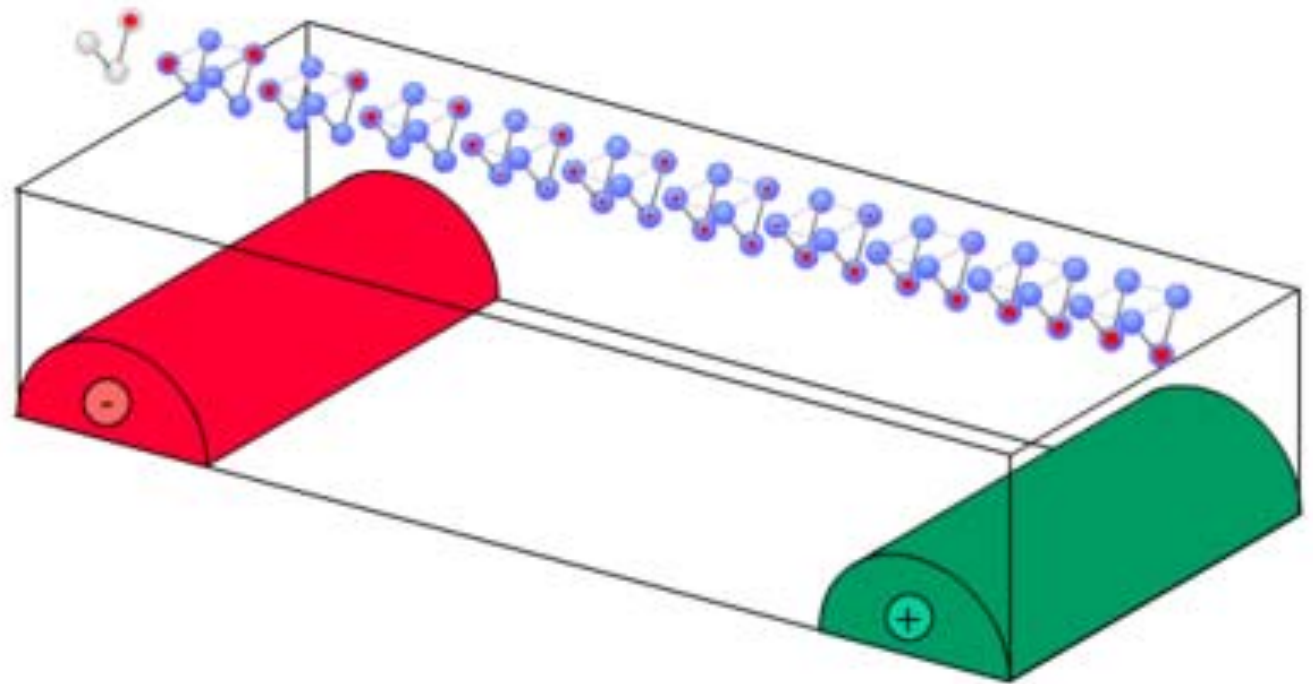
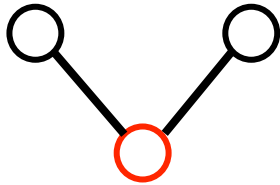
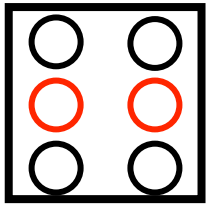


Top
View



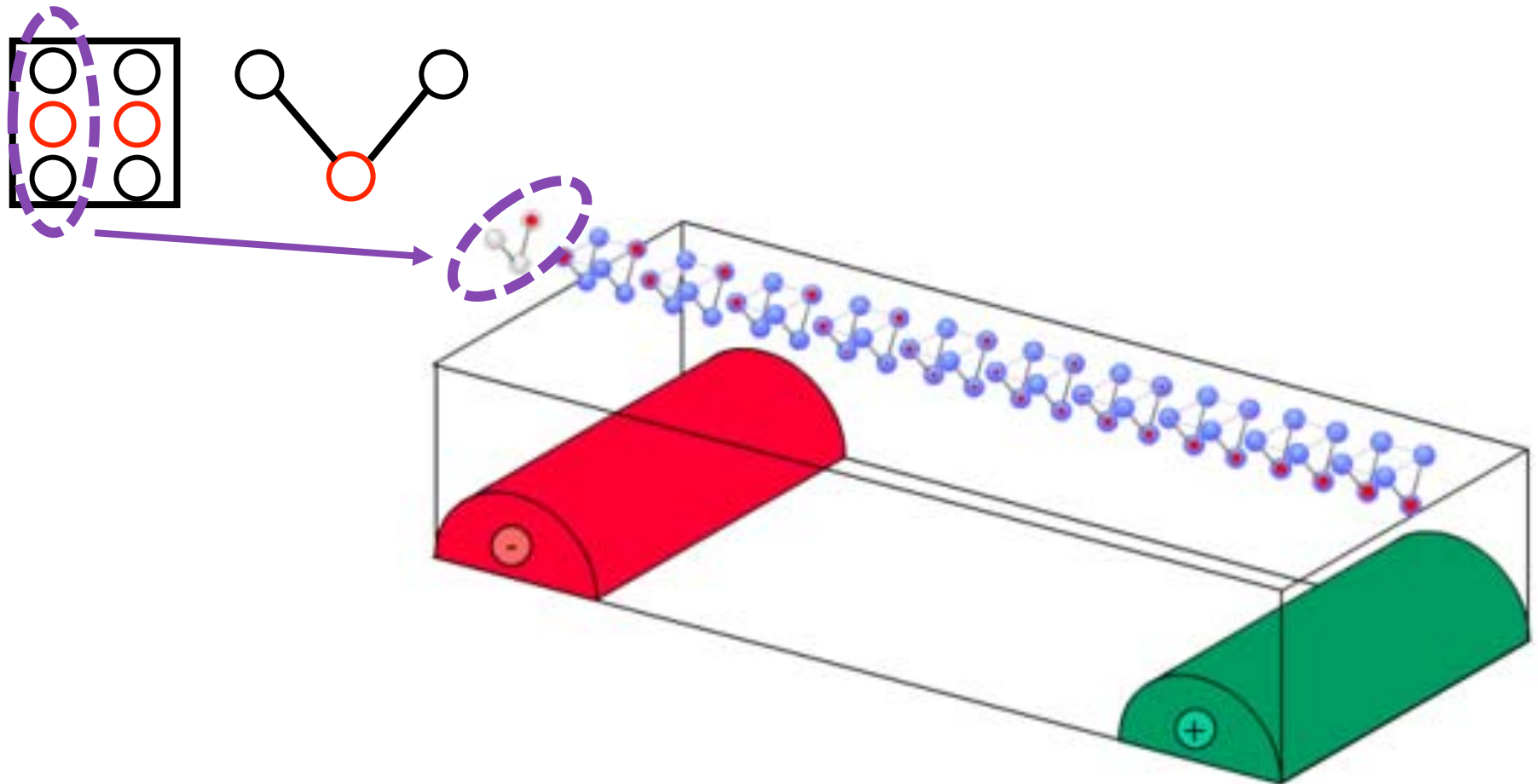
Side
View

Clocked QCA



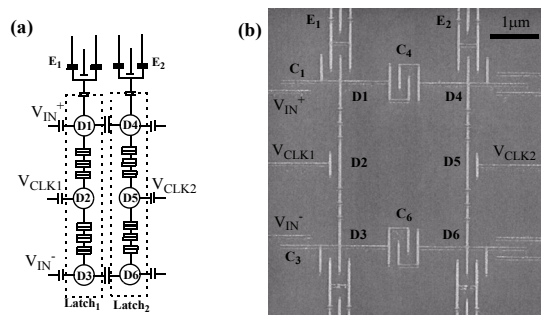
Lent, 2016.

Clocked QCA

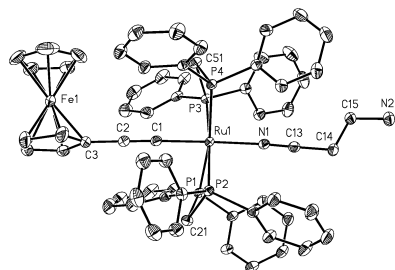


Lent, et.al, "Molecular Cellular Networks: A Non von Neumann Architecture for Molecular Electronics"
2016 IEEE International Conference on Rebooting Computing (ICRC), 2016.

The Devices

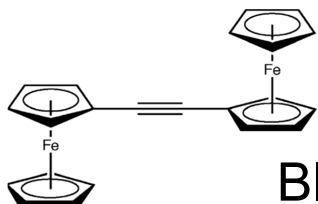


Clocked Shift Register (Orlov, 2002)



Li, 2003

Figure 3. Structure of the cation of $[trans-Ru(dppm)_2(C\equiv Cfc)(N\equiv CCH_2CH_2NH_2)][PF_6]$ (3) with 50% thermal ellipsoids (hydrogens omitted).



Blair, 2016

Diferrocenylacetylene (DFA)

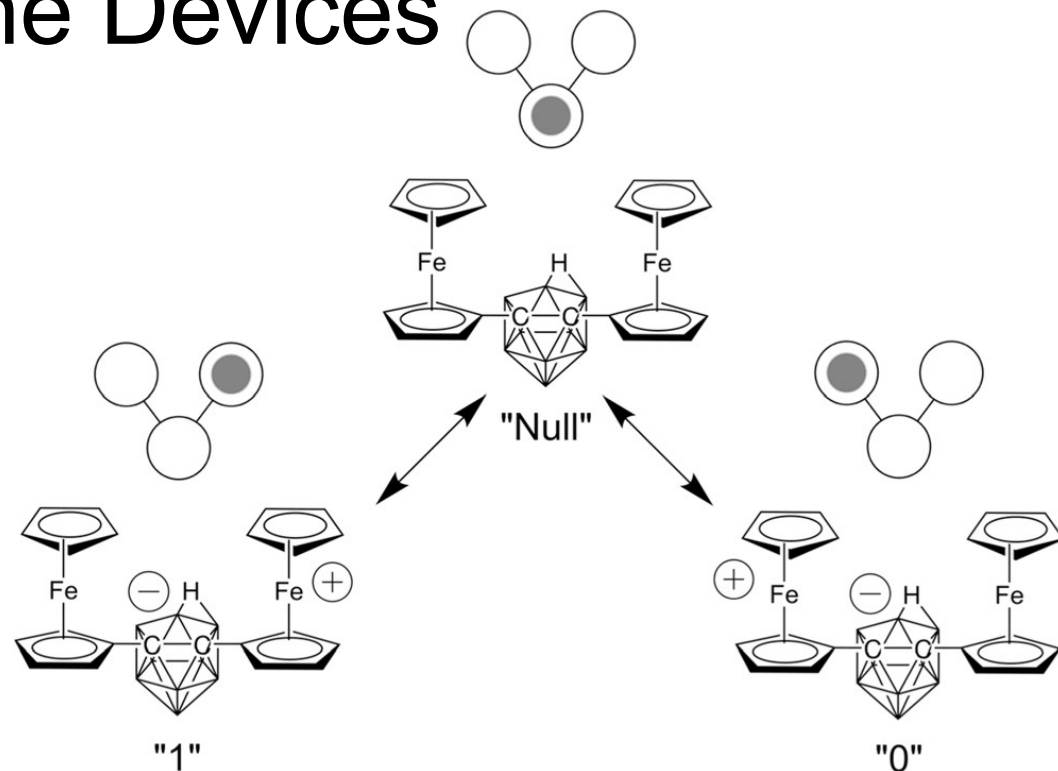
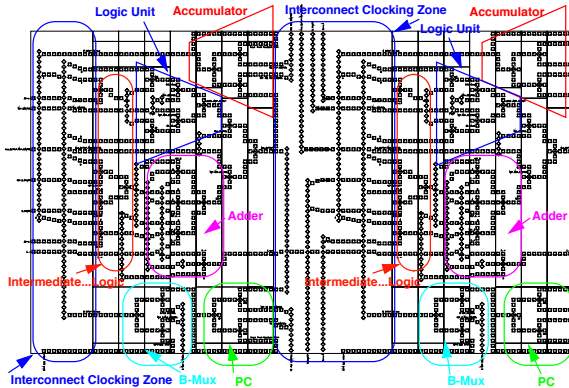


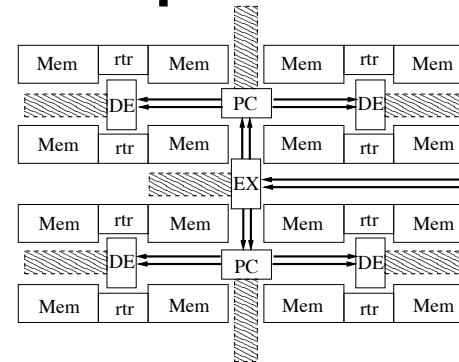
Figure 4. Bridge-mediated charge-transfer mechanism for the molecular switch $Fc^+FcC_2B_9^-$ (3a), highlighting the all-neutral null state intermediate.

Christie, 2015

Architecture: Proofs of Concept

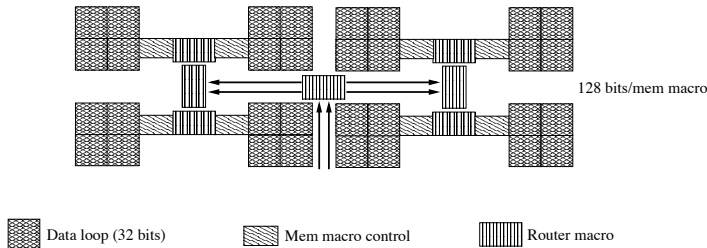


Traditional Processor
(Niemier 2004)

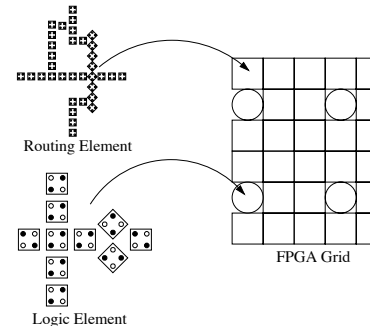


= Processing Logic
DE = Decode
PC = PC Inc
EX = Execute
rtr = Non-processing Router Macro
Mem = Memory Macro

Bouncing Threads
(Frost 2005)



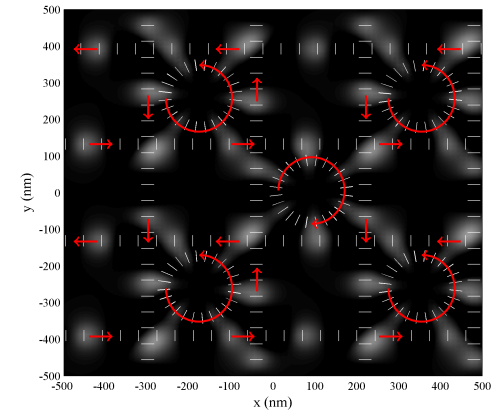
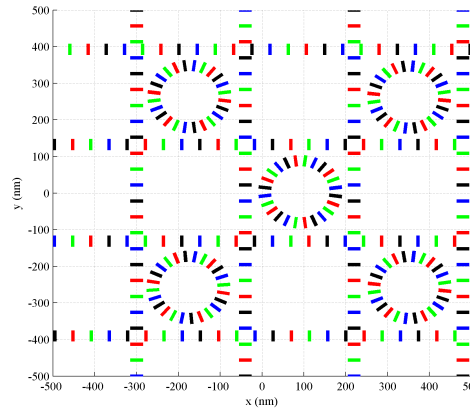
Traditional Memory
(Frost 2005)



FPGA
(Niemier 2002)

Clocking Floorplans

- Fabrication Issues
 - Structural Regularity
 - Temporal Regularity
- Architecture Issues
 - Layout = Timing
 - Flexible routing
 - Feedback

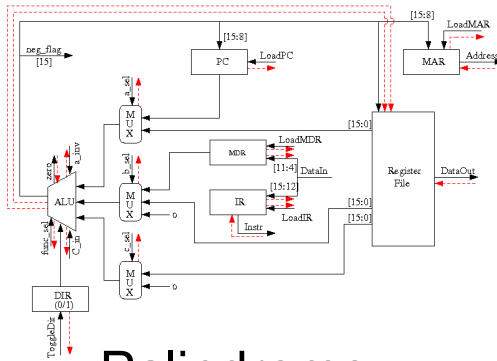


Blair, 2018

Physically Reversible Computing with QCA

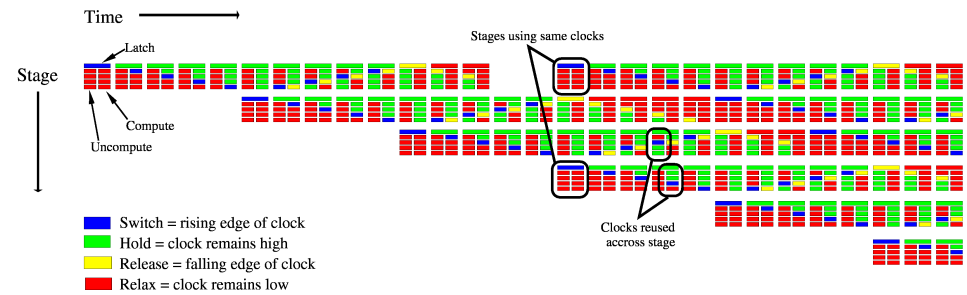
- Adiabatic: Slow compared to switching speed
 - Time for electron to hop across a molecule = very short
 - Clock speeds compared to that switching speed = very fast
- Pidaparthi and Lent: Exponential decrease in energy dissipation with adiabaticity (calculated)

Logically Reversible Computing with QCA

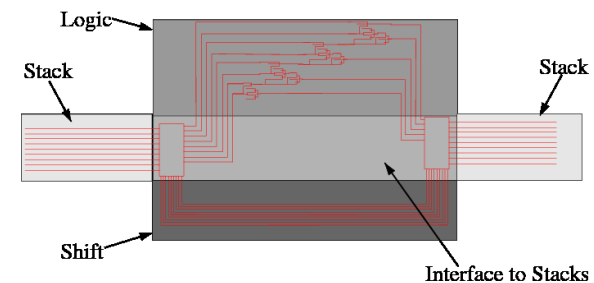


Palindrome -

Reversible at datapath/ISA level
(Frost-Murphy, 2009)



Retractable Cascade in QCA
(Frost-Murphy, 2006)



Collapsed Bennett

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