Kim Hazelwood
Senior Engineering Manager
Facebook

Awards and honors and year received (list--no more than *five* items):

- NSF CAREER Award, 2007
- Woodrow Wilson Foundation Career Enhancement Fellowship, 2008
- CRA-W Anita Borg Early Career Award, 2009
- MIT Tech Review Top 35 Innovators Under 35, 2010
- ACM SIGPLAN 10-Year Test of Time Award, 2015

Have you previously been involved in any CRA activities? If so, describe.

- I have been heavily involved in CRA-W activities over the years, and am passionate about the mission to broaden participation in computing. I have given numerous talks at the CRA-W Career Mentoring Workshops and Grad Cohort Summits on topics ranging including "Academia vs. Industry", "Internships: What, Why, How", "Work/Life Balance", and "How to Succeed in Graduate School".
- Because of my activities related to broadening participation in computing, mentorship, as well as my research, I received the Anita Borg Early Career Award, and most recently, was featured in the August 2016 CRA Bulletin.

List any other relevant experience and year(s) it occurred (list--no more than *five* items).

- CGO Steering Committee, 2010-2016
- Served on 35+ Conference/Workshop Program Committees, 2005-Present
- Hour Of Code Coordinator, San Jose Public Schools, 2014, 2015, 2016
- President of Yahoo Women in Tech, 2015
- Facebook Diversity Hiring Committee, 2016

Research interests: (list only)

- Computer Architecture
- Compiler Optimizations
- Data Center Server Architectures
- Performance Analysis and Tools
- Dynamic Binary Translation and Optimization

Personal Statement

Kim Hazelwood is an engineering manager at Facebook, whose research interests include computer architecture and performance analysis. She received her PhD from Harvard, and has since held positions including Associate Professor at UVa, Software Engineer at Google, and Director of Systems Research at Yahoo Labs, and she has held "tech diversity" leadership positions

at every institution. She is the recipient of an NSF CAREER Award, the Anita Borg Early Career Award, the MIT Technology Review "Top 35 Innovators under 35" Award, and the ACM SIGPLAN "10-Year Test of Time Award". She has authored 50+ conference papers and one book.

Brief Biography or CV
(Attached)

Kim Hazelwood, Ph.D.

(updated 12/2016)

3998 Payne Avenue, San Jose, California 95117, USA
Cell: 650.564.4454 ❖ Home: 408.900.9100 ❖ hazelwood.kim@gmail.com

EDUCATION

Harvard University, Cambridge, MA **2004**
Ph.D. in Computer Science
Dissertation: "Code Cache Management in Dynamic Optimization Systems"

North Carolina State University, Raleigh, NC **2000**
M.S. in Computer Engineering
Thesis: "Dynamic Optimization Infrastructures and Algorithms for IA-64"

Clemson University, Clemson, SC **1998**
B.S. with Honors in Computer Engineering (Minor: Mathematics)
Honors Thesis: "A Precision Analysis Agent for Reconfigurable Computing"

EXPERIENCE

Facebook, Menlo Park, CA **2015-Present**
Senior Engineering Manager
- Leading a team of performance engineers to drive the Facebook datacenter server and storage roadmap.

Yahoo, Sunnyvale, CA **2014-2015**
Director of Systems Research, Yahoo Labs
- Led the Systems Research Group on projects related to datacenter performance, power, and price. Projects leverage CPU analysis, GPU exploration, storage, and end-to-end user experience of large-scale applications including key-value store, video, images, and email.

Google, Mountain View, CA **2011-2014**
Software Engineer, Datacenter Platforms Performance and Secret Projects
- Performance and power analysis of large production workloads.
- Roadmapping and TCO analysis of datacenter hardware designs.
- Datacenter-scale benchmark development and maintenance.

Software Engineer, Gmail Performance
- Team of 3 reduced client-side memory consumption of Gmail by ~10x.

University of Virginia, Charlottesville, VA
Associate Professor of Computer Science with Tenure **2011-2012**
Assistant Professor of Computer Science **2005-2011**
- Taught courses in computer architecture, compilers, and virtual machines.
- Supported, managed, and mentored 12 graduate research assistants.
- Secured $3M in external research funding.
- Published over 35 articles and one book.

Intel Corporation, Hudson, MA
Faculty Consultant, Pin Dynamic Binary Instrumentation Group **2005-2011**
Post-Doctoral Researcher, Pin Dynamic Binary Instrumentation Group **2004-2005**
- Designed and implemented the code cache manager for Pin.
- Co-authored eight publications on Pin internals, receiving 2500 citations.
- Presented 10 tutorials on Pin at universities and academic conferences.
- Distributed Pin free of charge, with over 20,000 downloads.

IBM TJ Watson Research Center, Hawthorne, NY
Summer Intern, Jikes Research Virtual Machine Group — **2002**
- Designed and implemented an online inlining algorithm for Jikes RVM.
- Published results in CGO 2003. (60 citations)

Hewlett-Packard Laboratories, Cambridge, MA and Cupertino, CA
Summer Intern, DELI Project: Dynamic Execution Layer for Embedded Systems — **2001**
- Implemented and evaluated runtime optimizations for embedded systems.

Summer Intern, Dynamo Optimizer Group — **2000**
- Implemented the instruction internpreter for the x86 port of Dynamo.

Summer Intern, CarbonFIRE Adaptive Systems Group — **1999**
- Developed a random IA-64 instruction generator for nightly testing.

HONORS AND AWARDS

- ACM SIGPLAN 10-Year "Test of Time" Award, 2015.
- Named one of the "Top 35 Innovators under 35" by MIT Technology Review, 2010.
- Virginia Space Grant Consortium (VSGC) New Investigator Award, 2010. (Five Recipients per Year)
- Anita Borg Early Career Award, 2009. (One Recipient per Year Worldwide)
- Selected as 1 of 12 "World-Class Experts" for ACACES Summer School in Barcelona Spain, 2009.
- Woodrow Wilson Foundation Career Enhancement Fellowship, 2008. (20 Recipients Nationwide)
- Microsoft Secure and Scalable Computing Award, 2008. (7 Recipients Worldwide)
- National Science Foundation CAREER Award, 2007.
- FEST Distinguished Young Investigator Award, 2007. (4 Recipients per Year)
- Guest Speaker Presentations at Michigan, CMU, Harvard, MIT, UMass, Duke, UW, UCSB, Stanford, Clemson, Microsoft, CRA Workshop, Princeton, Intel Santa Clara, Google, Intel Hudson, Intel Beijing, IBM Research, Cornell, Princeton, NC State, Intel Hudson, UT Austin, Northeastern, Tufts
- Keynote Presentation – Local Support Partners (LSP) Annual Conference, 2007.
- Best Presentation Award, Code Generation and Optimization Conference, 2004.

BOOKS

- Kim Hazelwood. Dynamic Binary Modification: Tools, Techniques, and Applications. Morgan & Claypool Publishers. March 2011.

REFEREED CONFERENCE PAPERS

1. Svilen Kanev, Juan Pablo Darago, Kim Hazelwood, Parthasarthy Ranganathan, Tipp Moselely, Gu-Yeon Wei, and David Brooks. "Profiling a Warehouse-Scale Computer." International Symposium on Computer Architecture (ISCA), June 2015.
2. Svilen Kanev, Kim Hazelwood, David Brooks, and Gu-Yeon Wei, "Tradeoffs between Power Management and Tail Latency in Warehouse-Scale Applications". IEEE International Symposium on Workload Characterization, Raleigh, NC, October 2014.
3. Chris Gregg, Luther Tychonievich, Kim Hazelwood, James Cohoon. "Parallel Programming in Elementary School," Proceedings of the 43rd ACM Technical Symposium on Computer Science Education. Raleigh, NC. February 2012.
4. Kim Hazelwood. "Process-Level Virtualization for Runtime Adaptation of Embedded Software", 48th Annual ACM/EDAC/IEEE Design Automation Conference (DAC). San Diego, California, USA. June 2011.
5. Chris Gregg and Kim Hazelwood. "Where is the Data? Why You Cannot Debate GPU vs CPU Performance without the Answer," Int'l Symposium on Performance Analysis of Systems and Software (ISPASS). Austin, TX. April 2011.
6. Dan Upton and Kim Hazelwood. "Finding Cool Code: An Analysis of Source-Level Causes of Temperature Effects," International Symposium on Performance Analysis of Systems and Software (ISPASS). Austin, TX. April 2011.
7. Michelle McDaniel and Kim Hazelwood. "Performance Characterization of Mobile-Class Nodes: Why Fewer Bits is Better," Int'l Symposium on Performance Analysis of Systems and Software (ISPASS). Austin, TX. April 2011.
8. Apala Guha, Kim Hazelwood, and Mary Lou Soffa. "Balancing Memory and Performance through Selective Flushing of Code Caches," Compilers, Architectures, and Synthesis for Embedded Systems (CASES). Scottsdale, AZ. October 2010. (Acceptance rate: 41%)

9. Dan Upton and Kim Hazelwood. "Design of a Custom VEE Core in a Chip Multiprocessor," Proceedings of the 6th IEEE Symposium on Application Specific Processors (SASP). Anaheim, CA. June 2010. (35%)
10. Alex Skaletsky, Tevi Devor, Nadav Chachmon, Robert Cohn, Kim Hazelwood, Vladimir Vladimirov, Moshe Bach. "Dynamic Program Analysis of Microsoft Windows Applications," International Symposium on Performance Analysis of Software and Systems (ISPASS). White Plains, NY. April 2010. (34%)
11. Apala Guha, Kim Hazelwood, Mary Lou Soffa. "DBT Path Selection for Holistic Memory and Performance," in International Conference on Virtual Execution Environments (VEE). Pittsburgh, PA. March 2010. (27%)
12. Daniel Williams, Aprotim Sanyal, Dan Upton, Jason Mars, Sudeep Ghosh, and Kim Hazelwood. "A Cross-Layer Approach to Heterogeneity and Reliability," 7th ACM/IEEE International Conference on Formal Methods and Models for Co-Design (MEMOCODE). Cambridge, MA, USA. July 2009, pages 88-97. (35%)
13. Kim Hazelwood, Greg Lueck, and Robert Cohn. "Scalable Support for Multithreaded Applications on Dynamic Binary Instrumentation Systems," International Symposium on Memory Management (ISMM). Dublin, Ireland. June 2009, pages 20-29. (46%)
14. Arkaitz Ruiz-Alvarez and Kim Hazelwood. "Evaluating the Impact of Dynamic Instrumentation on Instruction Cache Performance," Int'l Symposium on Workload Characterization. Seattle, WA. Sept 2008. (34%)
15. Duane Merrill and Kim Hazelwood. "Exploring the Potential of Binary Trace Execution within Compile-Only JVMs," in Proceedings of the 2008 Annual ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments (VEE). Seattle, WA. March 2008, pages 41-50. (32%)
16. Steven Wallace and Kim Hazelwood. "SuperPin: Parallelizing Dynamic Instrumentation for Real-Time Performance," in Proceedings of the 5th Annual IEEE/ACM International Symposium on Code Generation and Optimization (CGO-5). Palo Alto, California, USA. March 2007, pages 209-217. (32%)
17. Apala Guha, Kim Hazelwood, Mary Lou Soffa. "Reducing Exit Stub Memory Consumption in Code Caches," in Proceedings of the High Performance Embedded Architectures and Compilers (HiPEAC). Ghent, Belgium. January 2007, pages 87-101. (29%)
18. Kim Hazelwood and Artur Klauser. "A Dynamic Binary Instrumentation Engine for the ARM Architecture," in Proceedings of Compilers, Architecture, and Synthesis for Embedded Systems (CASES). Seoul, Korea. October 2006, pages 261-270. (41%)
19. Kim Hazelwood and Robert Cohn. "A Cross-Architectural Framework for Code Cache Manipulation," in Proceedings of the 4th Annual IEEE/ACM Symposium on Code Generation and Optimization (CGO-4). New York, NY. March 2006, pages 17-27. (35%)
20. David Hiniker, Kim Hazelwood, Michael D. Smith. "Improving Region Selection in Dynamic Optimization Systems," in Proceedings of the 38th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-38). Barcelona, Spain. November 2005, pages 141-154. (20%)
21. C-K Luk, R Cohn, R Muth, H Patil, A Klauser, G Lowney, S Wallace, V Janapa Reddi, K Hazelwood. "Pin: Building Customized Program Analysis Tools with Dynamic Instrumentation," in the Conference on Programming Language Design and Implementation (PLDI). Chicago, IL. June 2005, pages 191-200. (21%)
22. Kim Hazelwood and David Brooks. "Eliminating Voltage Emergencies via Microarchitectural Voltage Control Feedback and Dynamic Optimization," in Proceedings of the 2004 ACM International Symposium on Low-Power Electronics and Design (ISLPED). Newport Beach, CA. August 2004, pages 326-331. (34%)
23. Kim Hazelwood and James E. Smith. "Exploring Code Cache Eviction Granularities in Dynamic Optimization Systems," in Proceedings of the 2nd Annual IEEE/ACM International Symposium on Code Generation and Optimization (CGO-2). Palo Alto, California, USA. March 2004, pages 89-99. (Best Presentation) (32%)
24. Kim Hazelwood and Michael D. Smith. "Generational Cache Management of Code Traces in Dynamic Optimization Systems," in Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-36). San Diego, California, USA. December 2003, pages 169-179. (26%)
25. Kim Hazelwood and David Grove. "Adaptive Online Context-Sensitive Inlining," in International Symposium on Code Generation and Optimization (CGO-1). San Francisco, CA, USA. March 2003, pages 253-264. (35%)
26. Kim Hazelwood and Thomas Conte. "A Lightweight Algorithm for Dynamic If-Conversion during Dynamic Optimization," in Proceedings of the 2000 ACM International Conference on Parallel Architectures and Compilation Techniques (PACT). Philadelphia, Pennsylvania, USA. October 2000, pages 71-80. (21%)
27. Kim Hazelwood, Walter Ligon, Greg Monn, Natasha Pothen, Ron Sass, Dan Stanzione, and Keith Underwood. "Creating Applications in RCADE," in Proceedings of the IEEE Aerospace Conference, Volume 2. Aspen, Colorado. IEEE Computer Society Press. March 1999, pages 337-349.
28. Brian Boysen, Nathan DeBardeleben, Kim Hazelwood, Walter Ligon, Ron Sass, Dan Stanzione, and Keith Underwood. "A Development Environment for Configurable Computing," in SPIE 3526: Configurable Computing Technology and Applications, Bellingham, Washington, USA. November 1998, pages 103-112.

JOURNAL PAPERS AND MAGAZINE ARTICLES

29. Svilen Kanev, Juan Pablo Darago, Kim Hazelwood, Parthasarathy Ranganathan, Tipp Moseley, Gu-Yeon Wei, David Brooks. "Profiling a Warehouse-Scale Computer", IEEE Micro's Top Picks in Computer Architecture Conferences. June 2016.
30. Apala Guha, Kim Hazelwood, and Mary Lou Soffa. "Memory Optimization of Dynamic Binary Translators for Embedded Systems," Transactions on Architecture and Code Optimization (TACO), Volume 9, Issue 3, September 2012.
31. Vijay Janapa Reddi, Simone Campanoni, Meeta Gupta, Kim Hazelwood, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "Eliminating Voltage Emergencies via Software-Guided Code Transformations," Transactions on Architecture and Code Optimization (TACO), August 2010.
32. Moshe Bach, Mark Charney, Robert Cohn, Tevi Devor, Elena Demikovsky, Kim Hazelwood, Chi-Keung Luk, Gail Lyons, Harish Patil, Ady Tal. "Analyzing Parallel Programs with Pin," IEEE Computer. March 2010.
33. Mojtaba Mehrara, Thomas Jablin, Dan Upton, David August, Kim Hazelwood, and Scott Mahlke. "Compilation Strategies and Challenges for Multicore Signal Processing," IEEE Signal Processing Magazine. Nov 2009.
34. Kim Hazelwood and Mohamed Zahran. "Challenges and Opportunities at All Levels: Interactions Among Operating Systems, Compilers, and Multicore Processors," ACM SIGOPS Operating System Review. Volume 43, Issue 2. April 2009.
35. Kim Hazelwood and Michael D. Smith. "Managing Bounded Code Caches in Dynamic Binary Optimization Systems," Trans. on Architecture and Code Optimization (TACO), Vol 3, Iss 3, Sep 2006, pages 263-294.
36. Jason Mars, Dan Upton, Kim Hazelwood. "Unobtrusive Reactive Prefetching: A Multicore Approach for Exploiting Hot Streams in Cache Misses," Under Review for Journal of Instruction-Level Parallelism (JILP).

REFEREED WORKSHOP PAPERS

37. Chris Gregg, Jonathan Dorn, Kim Hazelwood, and Kevin Skadron. "Fine-Grained Resource Sharing for Concurrent GPGPU Kernels," 4th USENIX Workshop on Hot Topics in Parallelism (HotPar). Berkeley, CA. June 2012.
38. Michelle McDaniel and Kim Hazelwood. "Runtime Adaptation: A Case for Reactive Code Alignment," Proceedings of the 2nd International Workshop on Adaptive Self-Tuning Computing Systems for the Exaflop Era (Exadapt). London, UK. March 2012.
39. Chris Gregg, Michael Boyer, Kim Hazelwood, and Kevin Skadron. "Dynamic Heterogeneous Scheduling Decisions Using Historical Runtime Data," Proceedings of the 2nd Workshop on Applications for Multi- and Many-Core Processors. San Jose, CA. June 2011.
40. Yair Lifshitz, Robert Cohn, and Kim Hazelwood. "Zsim: A Fast Architectural Simulator for ISA Design-Space Exploration," 3rd Workshop on Infrastructures for Software/Hardware Co-Design (WISH-3). Chamonix, France. April 2011.
41. Perhaad Mistry, Chris Gregg, Norman Rubin, David Kaeli, and Kim Hazelwood. "Analyzing Program Flow within a Many-Kernel OpenCL Application," 4th Workshop on General Purpose Processing on Graphics Processing Units (GPGPU-4). Newport Beach, CA. March 2011.
42. Derek Davis and Kim Hazelwood. "Improving Region Selection through Loop Completion," ASPLOS Workshop on Runtime Environments/Systems, Layering, and Virtualized Environments (RESoLVE). March 2011.
43. Balaji Dhanasekaran and Kim Hazelwood. "Improving Indirect Branch Translation in Dynamic Binary Translators," ASPLOS Workshop on Runtime Environments/Systems, Layering, and Virtualized Environments.. March 2011.
44. Chris Gregg, Jeff Brantley, and Kim Hazelwood. "Contention-Aware Scheduling of Parallel Code for Heterogeneous Systems," 2nd USENIX Workshop on Hot Topics in Parallelism (HotPar'10). June 2010.
45. Dan Upton, Kim Hazelwood, Greg Lueck, and Robert Cohn. "Improving Instrumentation Speed via Buffering," Workshop on Binary Instrumentation and Applications (WBIA). December 2009.
46. Marisabel Guevara, Chris Gregg, Kim Hazelwood, Kevin Skadron. "Enabling Task Parallelism in the CUDA Scheduler," in Workshop on Programming Models for Emerging Architectures. Raleigh, NC. Sept 2009.
47. Jason Mars, Daniel Williams, Dan Upton, Sudeep Ghosh, Kim Hazelwood. "Unobtrusive Reactive Prefetching: A Multicore Approach for Exploiting Hot Streams in Cache Misses," in Proceedings of the Workshop on Software and Hardware Challenges of Manycore Platforms (SHCMP). Beijing, China. June 2008.
48. Apala Guha, Kim Hazelwood, Mary Lou Soffa. "Code Lifetime-Based Memory Reduction for Virtual Execution Environments," in 6th Annual Workshop on Optimizations for DSP and Embedded Systems (ODES). Apr 2008.
49. Apala Guha, Jason D. Hiser, Naveen Kumar, Jing Yang, Min Zhao, Shukang Zhou, Bruce R. Childers, Jack W. Davidson, Kim Hazelwood, Mary Lou Soffa. "Virtual Execution Environments: Support and Tools," in NSF Next Generation Software Program Workshop. Long Beach, CA, USA. March 2007, pages 1-6.
50. Dan Upton and Kim Hazelwood. "Heterogeneous Chip Multiprocessor Design for Virtual Machines," in Software Tools for Multicore Systems. Palo Alto, CA. March 2007, pages 44-47.

51. Kim Hazelwood. "Tortola: Addressing Tomorrow's Computing Challenges through HW/SW Symbiosis," Boston Area Architecture Workshop, Kingston, RI, February 2006.
52. Kim Hazelwood and Michael D. Smith. "Characterizing Inter-Execution and Inter-Application Optimization Persistence," Workshop on Exploring the Trace Space for Dynamic Optimization Techniques. San Francisco, June 2003, pp. 51-58.
53. Kim Hazelwood and Michael D. Smith. "Code Cache Management Schemes for Dynamic Optimizers," 6th Workshop on Interaction between Compilers and Computer Architectures. February 2002, pp. 102-110.
54. Kim Hazelwood, Mark Toburen and Thomas Conte. "A Case for Exploiting Memory-Access Persistence," 2001 Workshop on Memory Performance Issues held in conjunction with ISCA. Gothenburg, Sweden, June 2001.

THESES AND TECHNICAL REPORTS

55. Jiayuan Meng, Dee A. B. Weikle, Kim Hazelwood. "ParaWeaver: Performance Evaluation of Programming Models for Fine-Grained Threads," University of Virginia Technical Report CS-2007-09, May 2007.
56. Kim Hazelwood. "Code Cache Management in Dynamic Optimization Systems." Ph.D. Thesis, Division of Engineering and Applied Sciences, Harvard University, May 2004.
57. Kim Hazelwood. "Dynamic Optimization Infrastructure and Algorithms for IA-64." Master's Thesis, Department of Electrical and Computer Engineering, North Carolina State University, June 2000.
58. Kim Hazelwood. "Feedback-Directed Query Optimization," Harvard Technical Report TR-03-03, Feb 2003.
59. Geetika Tewari and Kim Hazelwood. "Adaptive Web Proxy Caching Algorithms," Harvard University Technical Report TR-13-04, Feb 2004.
60. Nathan DeBardeleben, Stacey Dorsey, Kim Hazelwood and Jonathan Perry. "Next-Generation Software Configuration Management System," Senior Design Project, Clemson University, June 1998.

INVITED TALKS

- *Facebook Datacenters*, presented at UCSD and Harvard, November 2016.
- *Masters vs. PhD*, presented at CRA-W Grad Cohort, April 2016.
- *Industry vs. Academia*, panelist at CRA-W Grad Cohort, 2014.
- *Performance Analysis at Scale.* Guest Lecture at Stanford and EPFL Winter School. 2015, 2014, 2013.
- *A Case for Runtime Adaptation and Cross-Layer Integration*, presented at University of Versailles, Stanford University, UC Santa Barbara, Microsoft Research, University of Washington, Carnegie-Mellon University, Duke University, Massachusetts Institute of Technology, Harvard University, UMass Amherst, Princeton University. Spring 2010.
- *Ubiquitous Software: A Blessing and a Curse*, UVA Venture Summit. April 2010.
- *Advice from Early Career Faculty*, Panelist (with Dan Grossman and Chad Jenkins). Computing Research Association Career Mentoring Workshop. Washington, DC. February 2010.
- *Tortola: Addressing Tomorrow's Computing Challenges through Hardware/Software Symbiosis*, T100 Entrepreneurs Reception. Darden Business School. Charlottesville, VA. September 2007.
- *Should I Do An Internship?* CRA-W PLOSA Workshop for Women & Minorities, Washington, DC. 3/2009.
- *Getting Started on PL Implementation Research*, CRA-W/CDC Prog. Lang. Workshop, Austin, TX. May 2007.
- *What Every Architect Should Know About Dynamic Optimization*, CRA-W/CDC Computer Architecture Summer School, Princeton, NJ. July 2006.
- *What I Wish I'd Known in Graduate School*, CRA-W/CDC Distinguished Lectures, Austin, TX. December 2005.
- *Managing Bounded Code Caches in DynamoRIO.* IBM T.J. Watson Research Center, Hawthorne NY. February 2004; Intel Corporation, Hudson MA. January 2004.
- *Generational Code Cache Management*. Grace Hopper Celebration of Women in Computing, Chicago IL, October 2004; Harvard Industrial Partnership Workshop, November 2003.
- *Adaptive Online Context-Sensitive Inlining*. Harvard Industrial Partnership Workshop, Cambridge MA, November 2002; IBM TJ Watson Research Center, Hawthorne NY, August 2002.

PROFESSIONAL SERVICE

- Steering Committee Member: Code Generation and Optimization (CGO). 2010-2016.
- Program Co-Chair: USENIX Hot Topics in Parallelism (HotPar). 2013.
- Program Co-Chair: International Symposium on Code Generation and Optimization (CGO). 2010.
- Guest Editor: ACM SIGOPS Operating System Review, Special Issue on the Interaction among Compilers, Operating Systems, and Multicore Architectures. April 2009.

- Program Committees:
  - Int'l Symposium on Architectural Support for Programming Languages. & Operating Systems (ASPLOS) 2017, 2015, 2013.
  - Int'l Symposium on Microarchitecture (MICRO). 2014, 2009, 2008.
  - Int'l Symposium on Performance Analysis of Systems and Software (ISPASS). 2013.
  - Int'l Symposium on Code Generation and Optimization (CGO) 2012, 2010, 2007, 2006.
  - Int'l Symposium on High Performance Computer Architecture (HPCA). 2016, 2012, 2007.
  - Int'l Symposium on Computer Architecture (ISCA). 2017, 2012, 2011, 2010.
  - Int'l Conference on High-Performance and Embedded Architectures & Compilers (HiPEAC). 2011.
  - Int'l Symposium on Operating System Design and Implementation (OSDI). 2010.
  - Int'l Conference on Parallel Architectures and Compilation Techniques (PACT). 2009, 2006.
  - Int'l Conference for High-Performance Computing, Networking, Storage and Analysis (SC). 2009.
  - Int'l Conference on High-Performance Computing (HiPC). 2008.
  - Int'l Symposium on Parallel Architectures (ISPA). 2008.
  - Int'l Symposium on Programming Language Design and Implementation (PLDI). 2016, 2007.
  - Int'l Conference on Virtual Execution Environments (VEE). 2006.
  - Workshop on Architectural Support for Binary Translation (AMAS-BT). 2011, 2010, 2009, 2008.
  - Workshop on Parallel Execution of Sequential Programs (PESPMA). 2008.
  - Workshop on Binary Instrumentation and Applications (WBIA). 2005.
- Organizing Committees:
  - Tutorials Chair. Programming Language Design and Implementation (PLDI) 2009.
  - Web Chair. Workshop on Architectural Support for Binary Translation (AMAS-BT). 2008, 2009.
  - Student Poster Judge: Programming Language Design and Implementation (PLDI) 2007.
  - Publicity Chair. International Symposium on Computer Architecture (ISCA). 2006.
  - Web Chair. International Symposium on Microarchitecture (MICRO). 2003.
- National Science Foundation Review Panels: 2010, 2009, 2008, 2007, 2006.
  - Computer Systems Research (CSR).
  - High End Computing University Research Activity (HECURA).
  - Computing Research Infrastructure (CRI).
  - Foundations of Computing Processes and Artifacts (CPA).
- Outreach Activities for Women and Minorities in Computing:
  - CRA-W Graduate Cohort Speaker: 2014.
  - CRA-W/CDC Summer School (Women/Minorities). Speaker: 2006, 2007, 2012.
  - CRA-W PLOSA Workshop. Speaker: 2009.
  - Diversity Committee. Founding Member. Univ. of Virginia CS Department. 2007–2012.
  - Grace Hopper Celebration of Women in Computing. Panelist 2005, 2007.
  - UT Austin Distinguished Female Faculty Lecture Series. 2005.

FUNDING SOURCES

- Virginia Space Grant Consortium New Investigator Award (6/2010-5/2011) – sole PI
- National Science Foundation CSR CORE (5/2010-4/2013) – co-PI (33%) with S. Mahlke and D. August
- National Science Foundation CSR CORE (9/2009-8/2012) – PI with K. Skadron
- Anita Borg Early Career Award (6/2009) – sole PI
- National Science Foundation CSR-EHCS Grant (9/2008-8/2010) – co-PI with K. Whitehouse, M. L. Soffa
- National Science Foundation CAREER Award (5/2008-5/2013) – sole PI
- Microsoft Secure and Scalable Computing Award (7/2008-6/2011) – sole PI
- National Science Foundation CPA Grant (7/2008-6/2009) – PI (33%) with D. August, S. Mahlke
- Woodrow Wilson Foundation Career Enhancement Fellowship (7/2008-6/2009) – sole PI
- Semiconductor Research Consortium (4/2008-3/2011) – PI (33%) with D. August, S. Mahlke
- Google Research Award (12/2007) – sole PI
- National Science Foundation CSR-EHS Grant (9/2007-9/2009) – PI with co-PIs: K. Whitehouse, M. L. Soffa
- FEST Distinguished Young Investigator Award (7/2007) – sole PI

GRADUATE STUDENTS

- Dan Upton, Ph.D. in Computer Science. "Enabling Efficient Online Profiling of Homogeneous and Heterogeneous Multicore Systems". August 2011. (First position after graduation: Microsoft)
- Christopher Gregg, Ph.D. in Computer Engineering. "Contention-Aware Scheduling of Parallel Code for Heterogeneous Systems". August 2012. (First position after graduation: Tufts University)
- Apala Guha, Ph.D. in Computer Engineering. Co-advised with Mary Lou Soffa. "Memory Optimization of Dynamic Binary Translators for Embedded Platforms". June 2010. (First position after graduation: Intel)
- Michelle McDaniel, M.E. CS. "Assessing Opportunities for Reactive Code Realignment". May 2012.
- Jonathan Dorn, M.E. in CS. December 2012. Co-advised with Wes Weimer.
- Derek Davis, M.S. in CS. Thesis: "Improving Region Selection through Cycle Completion". August 2010.
- Balaji Dhanasekaran, M.E in CS. Project: Indirect Branch Handling in DBTs. August 2010.
- Blake Sheridan, M.E. CpE. Project: Performance Counter API for ARM. May 2009.
- Arun Thomas, M.E. CpE. Project: Memory-Efficient Dynamic Binary Translation. August 2008.

UNDERGRADUATE THESES ADVISED

- Julissa Campos, BS in Computer Science and Psychology. "Design and Implementation of a Data Collection System for Computer Science Diversity". Senior Thesis. May 2009.

TUTORIALS AND SHORT COURSES PRESENTED

- Performance Analysis in the Datacenter. Short course presented at the CUSO Winter School on Data-Centric Systems. Veysonnaz, Switzerland. January 2014.
- Using Pin for Compiler and Computer Architecture Research and Education. Tutorial presented at PLDI 2007, ASPLOS 2008, ISCA 2008, Intel Beijing, Northeastern University, Tufts University.
- Process Virtualization and Symbiotic Optimization. One week short course taught at ACACES Summer School. Barcelona, Spain. July 2009.

GRADUATE COURSES TAUGHT

- Compilers and Translation Systems. University of Virginia. Spring 2008. Spring 2010.
- Virtual Execution Environments. University of Virginia. Spring 2006, Spring 2007.
- Advanced Code Generation and Optimization. University of Virginia. Fall 2005.

UNDERGRADUATE COURSES TAUGHT

- Computer Architecture. University of Virginia. Fall 2009. Fall 2010.
- Introduction to Compilers. University of Virginia. Fall 2006. Fall 2007.

PUBLIC SOFTWARE RELEASES

- SuperPin: A Parallelized Implementation of the Pin Instrumentation Tool. Released March 2007.
- PinARM: A Dynamic Binary Instrumentation System for the ARM Architecture. Released October 2006.
- CodeCacheAPI: An API for Code Cache Introspection and Manipulation. Released March 2006.
- Pin: A Dynamic Binary Instrumentation System. Released with colleagues while at Intel. July 2004.

MEMBERSHIPS

- Association of Computing Machinery (ACM, ACM-W)
- Institute of Electrical and Electronic Engineers (IEEE)
- Women in Computer Architecture (WiCArch)

WORK STATUS

- United States Citizen