2021 BOARD NOMINEE

Josep Torrellas

Saburo Muroga Professorship of Computer Science, Computer Science
University of Illinois at Urbana-Champaign

CRA
Computing Research Association

Awards and Honors and Year Received

- IEEE Computer Society Harry H. Goode Memorial Award, 2021.
- Co-Leader, Intel Strategic Research Alliance (ISRA) Center on Computer Security, 2018.
- University of Illinois at Urbana-Champaign (UIUC) Campus Award for Excellence in Graduate Student Mentoring, 2017.
- Fellow of the American Association for the Advancement of Science (AAAS), 2016.
- IEEE Computer Society Technical Achievement Award, for ”Pioneering contributions to shared-memory multiprocessor architectures and thread-level speculation”, 2015.

Involvement in CRA Activities

- "From July 2016 to June 2019, I was an elected Member of the Board of Directors of CRA.
  * My main activity was to co-lead an initiative to improve computer science faculty recruiting, by creating an on-line CRA database of faculty candidates that can be accessed by CRA-member institutions. I would like to see this effort succeed.
  * As part of this effort, I co-organized a session on “Improving Faculty Recruiting in the Computing Community” in the 2018 Conference at Snowbird, July 2018.
- From January 2011 to June 2014, I was an elected Council Member of the Computing Community Consortium (CCC). My main activities included being a member of the Subcommittee on Visioning Activities. I acted a liaison for a Visioning Workshop from the Design Automation community.
- In April 2015, I attended the Leadership in Science Policy Institute Workshop in Washington DC.
- In May 2012, I co-edited a CCC Visioning white paper on “21st Century Computer Architecture”.
- In February 2010 and September 2010, I co-organized two CCC Visioning Workshops on Advancing Computer Architecture Research: “Failure is not an Option: Popular Parallel Programming” and “What Now in ILP Research?”.
  * These two workshops enabled the white paper listed in item 4), which in turn helped create the NSF CISE XPS program.

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Other Relevant Experience

1) Since October 2019, I have been Chair of IEEE Technical Committee on Computer Architecture (TCCA). I was Member of its Executive Committee before that. My main activities include:

* Organize and fund over 10 technical conferences yearly.
* Co-ordinate the funding and publicity of the Computer Architecture Letters
* Provide funds for students to travel to conferences
* Serve in the Steering Committees of conferences
* Successfully co-locate ACM PPoPP and IEEE HPCA for interdisciplinary interactions
* Create the HPCA Hall of Fame and the HPCA Conference Repository

2) Since May 2018, I have been a Member of the Board of Army Research and Development (BOARD), in the National Academy of Sciences.

3) Since September 2016, I have been a Member of the International Roadmap for Devices and Systems (IRDS). This is the organization that succeeds the International Roadmap for Semiconductors.

4) From 2011 to 2013, I was the Director of the Illinois-Intel Parallelism Center (I2PC), at UIUC. This was a center supported by Intel with $2M. It had 16 faculty. Main activities were:

* I organized the "2013 Illinois Symposium on Parallelism" in Urbana, Sept 2013 (http://i2pc.cs.illinois.edu/parworkshop/2013/schedule.html).

* I lead the preparation of a book with the research of all the faculty in the Center (http://iacoma.cs.uiuc.edu/iacoma-papers/Illinois_parallelism_book.pdf).

5) Graduated 43 Ph.D. students, 15 of which are now Professors at leading US universities, including MIT, Carnegie Mellon University, Cornell University, University of Washington, Georgia Tech, University of Southern California, and several others.

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Research Interests

Computer architecture, Parallel systems, Power- and security-aware computer architecture, Hardware resilience, Parallel software reliability.

Personal Statement

I am a professor of Computer Science at UIUC. In the past, I've been in the CRA Board, where I pushed an initiative to help faculty recruiting with a Candidate Database. I've served in the Computing Community Consortium(CCC), where I shepherded visioning research proposals. I co-organized two workshops on Advancing Computer Architecture Research, which helped create the NSF Exploiting Parallelism and Scalability(XPS) program. I am Chair of IEEE Technical Committee on Computer Architecture(TCCA), where I help nurture young researchers. At Illinois, I've been Director of the 16-faculty Intel Center for Parallelism. I've graduated 43 PhD students.

Josep Torrellas

Education

Aug 92	Ph.D. in Electrical Engineering, Stanford University. Dissertation: "Multiprocessor Cache Memory Performance: Characterization and Optimization". Advisor: John Hennessy.
Dec 87	M.S. in Electrical and Computer Engineering, University of Wisconsin - Madison.
Jun 86	B.S. in Electrical Engineering, Universitat Politecnica de Catalunya, Spain.

Appointments

Jun 18	-	pres.	Co-Leader, Intel Strategic Research Alliance (ISRA) Center on Computer Security, University of Illinois at Urbana-Champaign (UIUC).
Jan 16	-	pres.	Saburo Muroga Professor of Computer Science, UIUC.
Jan 11	-	pres.	Director, Center for Programmable Extreme-Scale Computing, UIUC.
Sep 11	-	Sep 13	Director, Illinois-Intel Parallelism Center (I2PC), UIUC.
Aug 02	-	pres.	Professor, Computer Science Department, UIUC.
Aug 02	-	Aug 09	Willett Faculty Scholar, Computer Science Department, UIUC.
Sep 07	-	Aug 10	Leader, University of Illinois OpenSPARC Center of Excellence, UIUC.
Feb 08	-	Aug 11	Computer Architecture Leader, Universal Parallel Computing Research Center (UPCRC), UIUC.
Aug 98	-	Aug 02	Associate Professor, Computer Science Department, UIUC.
May 98	-	Jan 99	Research Staff Member, IBM T.J. Watson Research Center, IBM Research (sabbatical).
Aug 92	-	Aug 98	Assistant Professor, Computer Science Department, UIUC.

Honors & Awards

2021	IEEE CS Harry H. Goode Memorial Award, February 2021.
2021	One Paper Selected and one Honorable Mention in IEEE Micro Top Picks from Computer Architecture.
2020	*Draco* System Call checking software upstreamed to Linux 5.11 as an extension of Seccomp.
2020	Best Paper Award, ASPLOS, March 2020.
2020	Two Papers Selected and one Honorable Mention in IEEE Micro Top Picks from Computer Architecture.
2020	Google Faculty Research Award.
2020	Keynote at the 2020 HPCA/PPoPP/CGO conferences.
2020	Research Highlight paper in Communications of the ACM (CACM).
2020	Cover article in IEEE Control Systems Magazine.
2019	Best Paper Award, 52nd International Symposium on Microarchitecture (MICRO), October 2019.
2019	Honorable Mention Paper, IEEE Micro Top Picks from Computer Architecture Conferences.
2017	Best Paper Nominee, International Conference on Parallel Architectures and Compilation Techniques (PACT).
2017	University of Illinois at Urbana-Champaign Campus Award for Excellence in Graduate Student Mentoring.
2016	Fellow of the American Association for the Advancement of Science (AAAS).
2015	IEEE Computer Society Technical Achievement Award, June 2015.
2015	Honorable Mention Paper, IEEE Micro Top Picks from Computer Architecture Conferences.
2014	Distinguished Paper Award, PLDI, June 2014.
2014	Best Paper Award Finalist, HPCA, Feburary 2014.
2013	Distinguished Speaker Award, IEEE International Conference on Application Specific Systems, Architectures and Processors (ASAP), June 2013.
2012	High-Impact Paper Award, International Conference on Computer Design (ICCD), October 2012. For "One of the 5 most cited papers in the first 30 years of ICCD (1983-2012)".
2010	ACM Fellow.
2009	Best Paper Award, 42nd International Symposium on Microarchitecture (MICRO), December 2009.
2009	Paper in IEEE Micro's Top Picks from Computer Architecture Conferences.
2009	Research Highlight paper in Communications of the ACM (CACM).
2009	Best Idea Award, Wild and Crazy Ideas Session, ASPLOS, March 2009.
2007	Paper in IEEE Micro's Top Picks from Computer Architecture Conferences.
2006	Best Paper Award, MICRO, December 2006.
2006	Paper in IEEE Micro's Top Picks from Computer Architecture Conferences.
2004	Paper in IEEE Micro's Top Picks from Computer Architecture Conferences.

2004	IEEE Fellow.
2003	Paper in IEEE Micro's Top Picks from Computer Architecture Conferences.
2002-9	Willett Faculty Scholar, UIUC.
2001	Best Paper Award, Fifth Workshop on Multithreaded Execution, Architecture, and Compilation.
2000	Senior Xerox Award for Outstanding Faculty Research, UIUC.
1997-00	IBM Partnership Award.
1997	C. W. Gear Outstanding Junior Faculty Award, UIUC.
1997	Junior Xerox Award for Outstanding Faculty Research, UIUC.
1995,6,8	Intel Research Council Award.
1994-9	Young Investigator Award, National Science Foundation.
1993-6	Research Initiation Award, National Science Foundation.

Graduated 43 Ph.D. Students (15 are Faculty at Top US Universities, of which 10 have received NSF CAREERs)

PhD students of Torrellas in faculty positions are: Dimitrios Skarlatos, 2020 (CMU); Mengjia Yan, 2019 (MIT); Nima Honarmand, 2014 (Stony Brook); Xuehai Qian, 2013 (USC); Ulya Karpuzcu, 2012 (Univ. of Minnesota); Abdullah Muzahid, 2012 (Texas A&M); Daniel Wonsun Ahn, 2012 (Univ. of Pittsburgh); Radu Teodorescu, 2008 (OSU); Luis Ceze, 2007 (Univ. of Washington); James Tuck, 2007 (NCSU); Jose Renau, 2004 (UC-SantaCruz); Milos Prvulovic, 2003 (Georgia Tech); Jose Martinez, 2002 (Cornell); Yan Solihin, 2002 (Univ. of Central Florida); Michael Huang, 2002 (Univ. of Rochester).

Main Professional Service

Nov 18 - pres.	Chair, The Institute of Electrical and Electronics Engineers (IEEE) Technical Committee on Computer Architecture (TCCA).
May 18 - pres.	Member, U.S. National Academies Board on Army Research and Development. – Co-organizer, workshops on "Machine Learning and High-Performance Computing", May 2020 and August 2020.
Mar 18	Co-organizer, NSF Visioning Workshop on "Inter-Disciplinary Research Challenges in Computer Systems for the 2020s", Williamsburg, VA. Workshop produced a report that was handed over to NSF and was published in the ACM Digital Library.
Sep 16 - pres.	Member, International Roadmap for Devices and Systems (IRDS) Applications Benchmarking Focus Team. – Successor of International Technology Roadmap for Semiconductors.
Jul 16 - Jun 19	Member, Board of Directors, Computing Research Association (CRA). Main activities included: – Co-lead an initiative to improve computer science faculty recruiting by creating an on-line database
Jan 11 - Jun 14	Council Member, The Computing Community Consortium (CCC), CRA. Main activities included: – Member of the Subcommittee on Visioning Activities
June 13	Chair and co-editor, "SIGARCH/TCCA's Recommended Best Practices for ISCA Program Chairs".
May 12	Co-editor, CCC white paper: "21st Century Computer Architecture, A Community White Paper".
Oct 10 - Oct 18	Member of the Executive Committee, IEEE TCCA.
Jul 05 - Oct 10	Chair, IEEE TCCA. Main accomplishments included: – Successfully co-located ACM PPoPP and IEEE HPCA for interdisciplinary interactions – Created the HPCA Hall of Fame and the HPCA Conference Repository – Created the HPCA conference Industrial Session
Feb 10 - Sep 10	Co-organizer of two CCC Visioning Workshops on Advancing Computer Architecture Research: "Failure is not an Option: Popular Parallel Programming" and "What Now in ILP Research?".
Dec 05	Participant in the CRA Visioning workshop: "Revitalizing Computer Architecture Research".
Jul 98 - Jul 05	Vice-Chair and Member of the Advisory Board, IEEE TCCA.

Designed Architectures

1. *QuickRec: A Hardware Prototype for Recording and Deterministically Replaying Multithreaded Programs in the Intel Architecture.* This prototype has been developed in collaboration with Intel, and is described in the QuickRec ISCA-2013 paper: http://iacoma.cs.uiuc.edu/iacoma-papers/isca13_1.pdf.

2. *Runnemede: An Chip Multiprocessor for Extreme-Scale Computing.* This manycore chip has been designed in collaboration with Intel, and is described in the Runnemede HPCA-2013 paper: http://iacoma.cs.uiuc.edu/iacoma-papers/hpca13_1.pdf.

Designed Software

1. *DRACO: A Linux Patch to Speed-up System Call Checking*. This is a patch in the official Linux distribution that checks system calls for security. December 2020.

2. *VARIUS and VARIUS-NTV: A Model of Process Variation*. This tool models within-die process variation and the resulting timing errors in manycores at a level suitable for microarchitects. June 2007. http://iacoma.cs.uiuc.edu/varius/index.html.

3. *SESC: A Simulator of Superscalar Multiprocessors and Memory Systems with Thread-Level Speculation Support*. SESC is a multiprocessor simulator package with support for thread-level speculation. June 2005. http://sourceforge.net/projects/sesc.

4. *Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors*. Scal-Tool is a public-domain tool that is available through the NCSA software repository. May 1999.

5. *Augmint: A Multiprocessor Simulation Environment for Intel x86 Architectures*. Augmint is a multiprocessor tracing and evaluation package that runs on Intel x86 machines. December 1995. http://iacoma.cs.uiuc.edu/augmint.html.

Publications

- About 300 publications
- Google Scholar: https://scholar.google.com/citations?user=zdnAkgsAAAAJ&hl=en with **h-index = 65**
- Ranking of Torrellas in various Computer Architecture Halls of Fame:
  Aggregated Computer Architecture Hall of Fame (top tier conferences ISCA, MICRO, HPCA, and ASPLOS): #2
  ISCA Hall of Fame: #2
  HPCA Hall of Fame: #1
  MICRO Hall of Fame: #5
  ASPLOS Hall of Fame: #5
- Five publications:

1. Antonio Franques, Apostolos Kokolis, Sergi Abadal, Vimuth Fernando, Sasa Misailovic, and Josep Torrellas, *WiDir: A Wireless-Enabled Directory Cache Coherence Protocol*, International Symposium on High-Performance Computer Architecture (HPCA), February 2021.

2. Zirui Neil Zhao, Houxiang Ji, Mengjia Yan, Jiyong Yu, Christopher W. Fletcher, Adam Morrison, Darko Marinov, and Josep Torrellas, *Speculation Invariance (InvarSpec): Faster Safe Execution Through Program Analysis*, International Symposium on Microarchitecture (MICRO), October 2020.

3. Apostolos Kokolis, Thomas Shull, Jian Huang, and Josep Torrellas, *P-INSPECT: Architectural Support for Programmable Non-Volatile Memory Frameworks*, International Symposium on Microarchitecture (MICRO), October 2020.

4. Zhangxiaowen Gong, Houxiang Ji, Christopher W. Fletcher, Christopher J. Hughes, Sara Baghsorkhi, and Josep Torrellas, *SAVE: Sparsity-Aware Vector Engine for Accelerating DNN Training and Inference on CPUs*, International Symposium on Microarchitecture (MICRO), October 2020.

5. Dimitrios Skarlatos, Qingrong Chen, Jianyan Chen, Tianyin Xu, and Josep Torrellas, *Draco: Architectural and Operating System Support for System Call Security*, International Symposium on Microarchitecture (MICRO), October 2020.